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RECONFIGURABLE IMPLEMENTATION OF QAM DEMODULATOR IN AN FPGA

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***Abstract*— In this project, an efficient all-digital demodulator in digital communication receivers is proposed and implemented on a reconfigurable hardware platform in order to compensate timing and carrier phase offset. In the proposed design, a feedforward architecture which has better stability and performance than traditional feedback architectures is used in the timing synchronization loop. To mitigate the problem of oversampling rate of feedforward synchronizer, an innovative parallel demodulator architecture is presented which is optimized for high speed transmissions. This proposed architecture results in asynchronous data sampling where there is no need to adjust sampling rate of the analog to digital converter with an external feedback. To achieve good stability conditions in the presence of loop delay in carrier recovery loop, an appropriate compensation method is utilized. Since the delay compensation technique is applied, the proposed architecture is well suited for VLSI implementations. In this project a numerically controlled oscillator with reduced lookup table is used to generate sine and cosine waves. The proposed architecture is used to implement QAM digital communication receiver on a Xilinx FPGA platform achieving higher clock rate. Implementation results show that our design has a good performance for different modulation orders as well as excellent robustness against loop delays and variations in the loop.**

***Index Terms*— carrier recovery loop, numerically controlled oscillator, direct digital synthesizer, matched filter.**

I. INTRODUCTION

This paper describes a new all-digital high-throughput timing and carrier synchronizer which has not only a good accuracy in estimation but also a good robustness against loop delay. In the proposed design, a feedforward timing synchronizer with oversampling rate is employed which induces better robustness and performance than feedback ones. In order to compensate the effect of oversampling in feedforward architectures, parallelization and pipelining methods are applied for implementation of various units. By utilizing these optimizations, clock frequency of each sub-system is increased and the design of high speed digital modems is simplified. The effect of loop delay is compensated, by appropriate modeling of carrier recovery loop. This technique provides a robust and high throughput architecture which can function optimally where some internal filters and optimization methods such as pipelining with large delays are needed. The lock-in range of this design is increased by using phase unwrapper block which can extend maximum detectable phase of the estimator. It is worth mentioning that the proposed architecture is fully digital and asynchronous with the received which helps in solving the problem of iteration bound, and is frequently used in high-speed communication.

High performance of hardware systems and flexibility in design and implementation are required for the development of mobile and portable communications. In such situation, silicon technology is one of the best choices which allow us to produce high execution, high integrated density and dedicated purpose integrated circuit(IC). At present FPGAs and ASICs are playing a vital role in designing, simulating, testing and implementing the new communication techniques. Moreover system level design and implementation is possible due to tools like system generator which facilitates testing algorithms,modifying designs as per the requirement very easily. Compared to ASIC, FPGA has simpler development cycle, low initial cost and are more flexible. The development in the modulation techniques had been witnessed since last two decades which demands reliable transmission of information with higher data rate. Due to high noise immunity, digital modulation techniques have created an interest. Modulation scheme such as QAM is one of the widely used modulation techniques in cellular communication because of its high efficiency in power and bandwidth.8-QAM (Quadrature Amplitude Modulation) is a kind of digital modulation scheme which transmits 3 bits per symbol on two orthogonal carriers; one in phase and the other one is in quadrature phase. Hence the data rate is increased. The hardware behavior of modulator was described using Verilog which is simpler than VHDL. Verilog has structured top-down approach which is independent of device and technology. It has fast switch level simulation and is portable between different tools and platforms.

QAM (quadrature amplitude modulation) is a method of combining two amplitude-modulated (AM) signals into a single channel, thereby doubling the effective bandwidth. QAM is used with pulse amplitude modulation (PAM) in digital systems, especially in wireless applications. In a QAM signal, there are two carriers, each having the same frequency but differing in phase by 90 degrees (one quarter of a cycle,

from which the term quadrature arises). One signal is called the Isignal, and the other is called the Q signal. Mathematically, one of the signals can be represented by a sine wave, and the other by a cosine wave. The two modulated carriers are combined at the source for transmission. But in this system a different algorithm is used in which the different carriers are stored in LUT and are multiplexed to output according to the message signal.

A. OBJECTIVE

High speed digital communication receivers suffer from some destructing effects like phase noise, Doppler, channel effects, local oscillator mismatching, etc. Hence, the presence of an appropriate synchronizer in receivers is inevitable. Several paths have been taken to overcome these problems. A proper architecture is selected based on maximum acceptable transmission rate, transmission media, expected performance, etc. On the other hand, many of the relevant publications have focused on reconfigurable hardware platforms for implementing synchronizers at the receivers. FPGAs are used for implementing both feedforward and feedback structures in clock and carrier synchronizers. Feedforward architectures usually are more stable and have better performance and rapid synchronization acquisition than their feedback counterparts. However, the main drawback of these architectures is their need for high sampling rate to estimate timing or phase offsets.

II. EXISTING SYSTEM

A Design and implementation of high throughput, robust, parallel qam demodulator in digital communication receiver

In this system to increase the rate of the receivers, some methods such as pipelining can be used. These methods introduce new delay elements in the loop and lead to instability problems. In synchronization loops, excess loop delay is an undesirable parameter and it should be compensated. Consequently, any reduction in the loop delay can improve the synchronization loop performance. The two carriers are named I and Q, in-phase and quadrature, and are usually a cosine (I) and sine (Q) wave due to their 90_ phase shifted relation to each other. The finite number of amplitude steps that the I and Q can be adjusted to implements different types of QAM modulations. This comes from each of the two carriers having two selectable amplitude levels and can thus represent one bit each, and together two bits. If the number of amplitude steps are increased to four the data represented by each point is four bits. By increasing the number of selectable amplitude steps, and thus the number of constellation points, more data can be represented by each point and thus a higher transmission rate can be achieved and the loss of SNR.

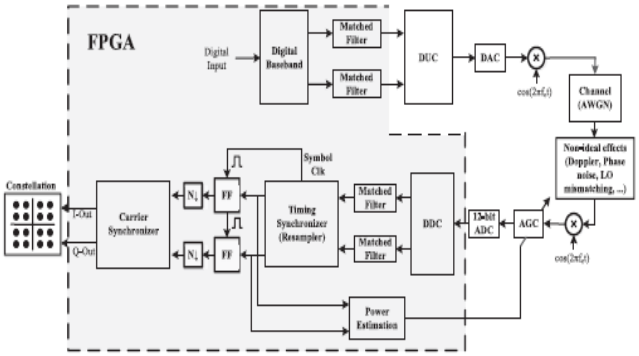

Fig. 1 Parallel QAM demodulator

III. PROPOSED SYSTEM

The block diagram of the final implemented system is shown in Fig. 2. In the implemented receiver, intermediate frequency (IF) sampling is carried out at the first stage using digital down conversion (DDC) in the digital domain. This unit consists of a DDS and two consecutive filters. Then, after passing the signal through SRRC filters, clock and carrier synchronization is performed on the received signal. The post-synthesis results show that the proposed architecture clocks at 612 MHz. In the proposed system, timing synchronization is performed before carrier synchronization because of non-sensitivity to phase and frequency in TED.

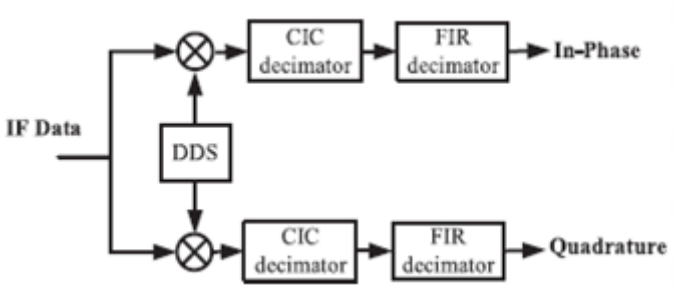

Fig.2 Block Diagram Of Proposed Method

A. A. Carrier recovery loop

The Feedback clock and carrier recovery loops can be modeled similar to PLL structures. The estimator is playing the role of phase detector (PD) in PLLs and can be modeled using S-curve characteristic. Therefore, the effect of this block is simplified to a gain. Moreover, loop filter (LF) is modeled as F(z) and timing control unit (TCU) or numerically control oscillator (NCO) is modeled as an integrator which integrates the output frequency. Similarly, the input phase can be obtained by integrating the input frequency using Hi (z). In Fig. 3 the effect of quantization noise is modeled by zero-mean uniform distributed random noise v(n) and the effects of phase noise and other external sources of noise are modeled by zero-mean Gaussian noise w(n) with varianceσ2w.

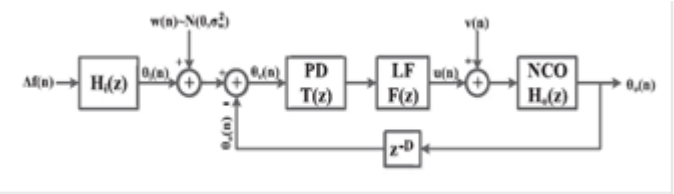

Fig3. Modeling of carrier recovery loop

The modification in the proposed system is made on the direct digital synthesizer block. Direct digital synthesis (DDS) is a powerful technique used in the generation of radio frequency used in the generation of radio frequency signals for use in radio receivers. The block diagram of DDS is shown in fig 4

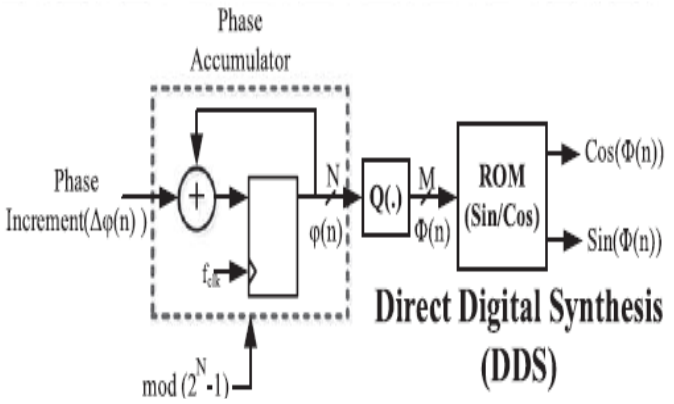

Fig.4 DDS unit

The synthesizer operates by storing various points in the form of waveform. The digital number representing the phase is given in the phase accumulator. The number held here corresponds to the phase and is increased at regular interval. Phase accumulator is basically a form of counter. When it is clocked it adds a preset number to the one already held. When it fills up, it resets and starts counting from zero again. Once phase has been determined it is necessary to convert this into a digital representation of the waveform. This is accomplish using a waveform map. This is a memory which stores a number corresponding to the voltage required for each value of phase on the waveform. In the case of a synthesizer of this nature it is a sine look up tables as a sine wave is required. In most cases the memory is read only memory or programmable read on only memory. This contains a vast number of points on the waveform. A very large number of points is required so that the phase accumulator can increment by a certain point to set the required frequency. The proposed system uses numerical controlled oscillator with reduced lookup tahle which reduces the number of points stored in ROM memory. The look up tables is used to store sample points for the generation of carrier signals. The carrier with different phases is obtained by changing the order in which the points are stored.

The external input is the message signal for the QAM modulator provided from a function generator. The external signal frequency has an upper limit depending on the number of points in the look up table and the clock frequency. The control block is used to synchronize the operation of the entire modulator section. The FPGA board has an inbuilt clock of 4.09 MHz and it is used as the control signal. The look up table (LUT) is used to store the sample points for the generation of carrier signals. The proposed system requires eight look up tables. Among these look up tables four of them consist of carrier signal of a particular amplitude in four different phases (45,135,225,315). Similarly, the rest consist of carrier signal of different amplitude. The carriers with different phases are obtained by changing the order in which the points are stored in the LUT. The sample points are calculated based on an equation and the number of sample points can be altered. As the number of sample points stored in the look up table increases the precision of the carrier wave generated increases. The frequency of the carrier signal generated will dependent on the clock frequency and the number of sample points, i.e. the clock frequency divided by the number of sample points in the look up table.

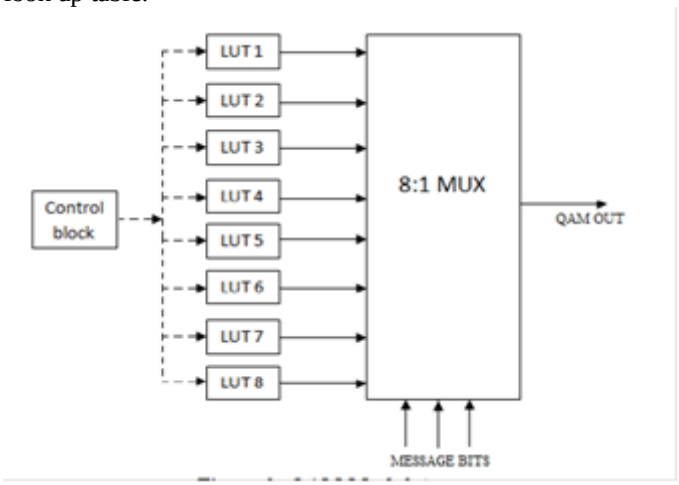

Fig5 Modified system

A 8:1 Multiplexer is used to facilitate the switching of the carrier signals to the output. The select line which controls the multiplexing action is the data input which is provided from a function generator. While performing offline modulation the output of a random sequence generator can be connected to the select line.

IV. SIMULATION RESULTS

The results show that the proposed scheme has higher maximum frequency and throughput compared to all reported VLSI implementations where the speed reaches up to 150 Msps for M-QAM modulation. In terms of area, the proposed design consumed more resources compared to other conventional architectures due to its efficiency in speed and flexibility in performing different orders of modulations.

A. Timing Summary:

- Maximum combinational path delay: 20.145ns
- Total memory usage is 255144 kilobytes

Table 1.1Device utilization summary

Slice Logic Utilization	Used	Available
Number of Slice LUTs	73	9112
Number used as Logic	73	9112
Slice Logic Distribution	Used	Available
Number with an unused Flip Flop	73	73
Number with an unused	0	73
LUT Number of fully used LUT-FF pairs	0	73
IO Utilization	Used	Available
Number of bonded IOBs	97	232

CONCLUSION

In this project, an efficient implementation of timing and carrier synchronizers for a coherent demodulator is proposed. Employing feedforward architecture in timing recovery and carrier recovery circuit has improved system robustness against delays in the loop. The system uses an LUT for carrier generation. By using LUT speed of the system increases and area utilized by the device can be reduced. The system offer good performance and stability than existing systems. The hardware behavior of demodulator was described using Verilog which is simpler than VHDL.Verilog has structured top-down approach which is independent of device and technology. It has fast switch level simulation and is portable between different tools and platform. . Implementation results show that our design has a good performance for different modulation orders as well as excellent robustness against loop delays and variations in the loop.

ADVANTAGES

- Lowers the power consumption.
- Enabling further voltage reduction.
- Lowest delay and PDP.
- Better candidate for high-speed low-energy applications.

APPLICATIONS

- Used in high speed communication.
- Used in satelitte communication.

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