International Journal of Technical Research and Applications e-ISSN: 2320-8163,
www.ijtra.com Volume 3, Issue 4 (July-August 2015), PP. 80-82

POD-PWM BASED CAPACITOR CLAMPED MULTILEVEL INVERTER

S. Devaraj, Dr. Anitha G S
Dept. of Electrical and Electronics Engg.
RV College of Engineering
Bengaluru, India
devaraj.sakaray@gmail.com

***Abstract*—Multilevel inverters play a crucial part in the areas of high and medium voltage applications. Among the three main multilevel inverters used, the capacitor clamped multilevel inverter(CCMLI) has advantage with respect to voltage redundancies. This work proposes a switching pattern to improve the performance of chosen H-bridge type CCMLI over conventional CCMLI. The PWM technique used in this work is Phase Opposition Disposition PWM(PODPWM). The performance of proposed H-bridge type CCMLI is verified through MATLAB-Simulink based simulation. It has been observed that the THD is low in chosen CCMLI compared to conventional CCMLI.**

***Index Terms*—Multilevel inverter, Phase Opposition Disposition- PWM(POD-PWM), CCMLI**

I. INTRODUCTION

The Multilevel voltage source converter topologies are the best suited for medium and high voltage applications in the industries. There are three main topologies of multilevel voltage source inverters [1–5]: neutral point clamped (NPC), capacitor clamped (CC) and cascaded H-bridge (CHB). The Capacitor Clamped topology [6] allows the conventional inverter to produce higher output voltages by using standard low-voltage switching devices available in the market, controlling the real and reactive power flow easily.

For the modulation of multilevel inverters, carrier-based modulation techniques are commonly used. Carrier-based modulation techniques are mainly divided into two types [1,2]: phase-shifted carrier pulse width modulation (PSC-PWM) and level-shifted carrier PWM (LSC-PWM). LSC-PWM, which is also called sub-harmonic PWM (SH-PWM), can be classified again into the following three subgroups based on the phase disposition of the carriers: phase disposition (PD), phase opposite disposition (POD) and alternative POD[7,8]. All of these subgroups differ in the way the carriers are displaced. The PSC-PWM is normally used for CHB inverters However, the Total Harmonic Distortion(THD) of output current with the PSC-PWM is worse than that of the LSC-PWM, especially under low-modulation index (MI) regions. On the other hand, LSC-PWM methods are generally applied to the CC and NPC inverters, which are based on amplitude shifts between carriers. In this work, POD PWM technique is used.

II. MULTILEVEL INVERTER

Figure 1 shows a conventional single phase five level CCMLI. One of the main advantages of CCMLI when compared to NPC topology is that single capacitor substitutes two diodes which results in simplification of the circuit and reduction of overall losses. CCMLI provides better voltage balancing across the clamping capacitors. To produce 'n' levels of output voltage, CCMLI requires (n-1)*(n-2)/2 number of clamping capacitors per phase leg and (n-1) main dc bus capacitors. So, a conventional single phase five level CCMLI consists of 6 clamping capacitors and 4 dc bus capacitors.

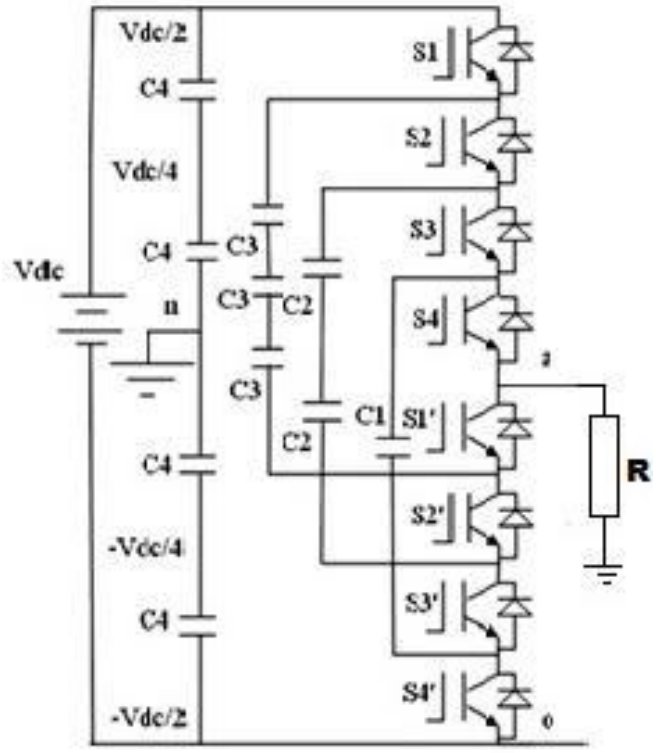

Fig 1.Conventional single phase five level CCMLI

The central point of the four dc bus capacitors can be referred as neutral point. The switches have been grouped into four pairs (S1, S1'), (S2, S2'), (S3, S3') and (S4, S4'). The switches in each pair are complementary to each other. So, if S2 is OFF, S2' will be ON and vice-versa. All the clamping capacitors have the same value.

Figure 2 shows the chosen H-bridge type CCMLI. In this paper, a single phase five level symmetric CCMLI uses a switching method in such a way that the number of clamping capacitors is reduced. We can observe from figures 1 and 2 that the number of clamping capacitors is reduced from 6 to 2 which reduces the cost, space and size of the multilevel inverter. This topology assures low total harmonic distortion(THD). The table 1 shows the comparison of devices used in conventional and chosen CCMLI.

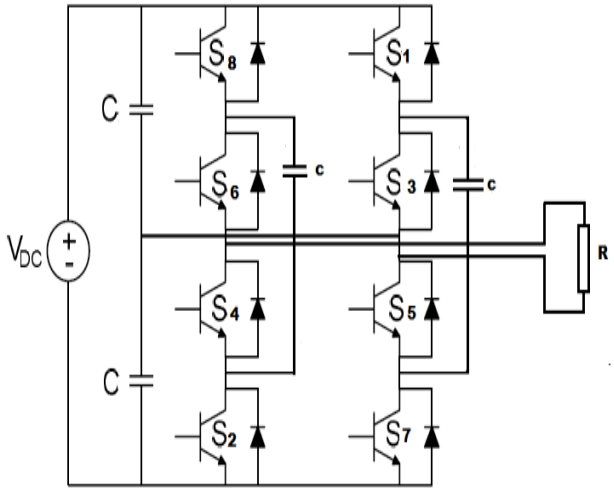

Fig 2.Chosen H-bridge type CCMLI

Type of MLI	Conventional FCMLI	Chosen FCMLI
Main power devices	8	8
Main diodes	8	8
Clamping capacitor	6	2
DC bus capacitors	4	2
No. of leg	1	2

Table-1 Comparison: conventional and chosen CCMLIs

III. PHASE OPPOSITION DISPOSITION PWM TECHNIQUE

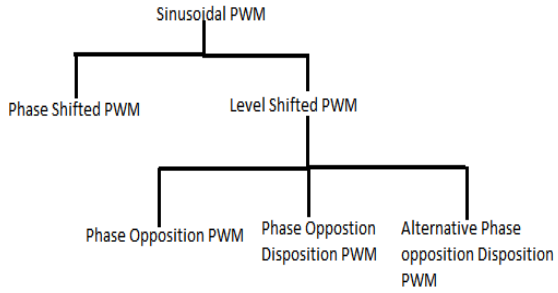

Fig 3. Classification of modulation techniques

As figure 3 shows, the sinusoidal PWM is broadly divided into level shifted PWM and phase shifted PWM. Level shifted PWM is again divided into three sub-categories-namely Phase Opposition Disposition PWM(POD PWM) , Alternative Phase Opposition Disposition PWM(APOD PWM) and Phase Disposition PWM(PD PWM) . This work has been carried out by using POD PWM technique.

A. POD PWM:

In five level inverter, four carrier signals are used and the following points explain about POD PWM.

The phase opposition disposition has all carriers at the same frequency with adjustable amplitudes. The only difference that it has with PD-PWM is that it has carriers above zero level reference in phase among them but in opposition, usually 180 degree phase shifted those of below

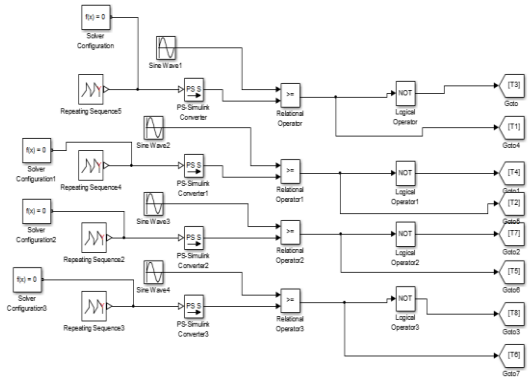

Fig 4. PWM generation using SIMULINK developed for PODPWM technique

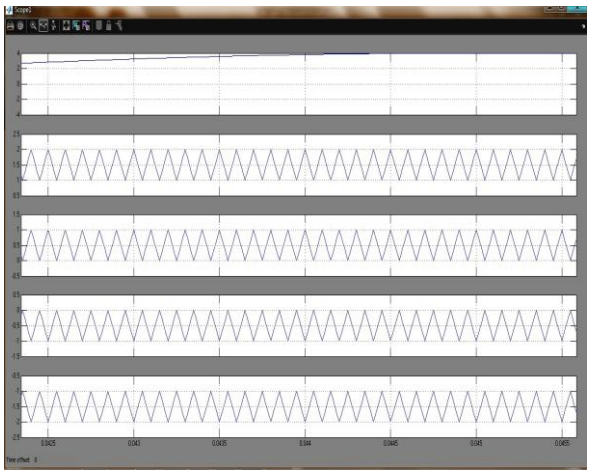

Fig 5. The carrier signals and the modulating signals

Table 2. Simulation parameters values

Parameter	Value
DC input voltage	220V
Flying capacitor	220uF
Carrier frequency	1100Hz
Load	100 Ohms

IV. OPEN LOOP SIMULATION

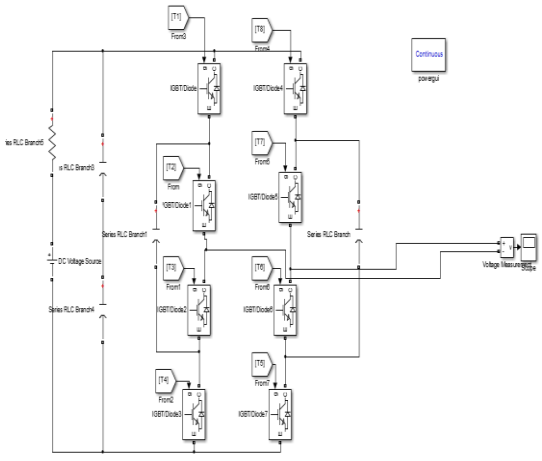

Fig 6. Open loop Simulink model

Using MATLAB tool, open loop circuit is modelled and simulated in Simulink. The parameters or values of the components used in the simulation are shown in table 2.

The simulation results are shown in the following figures:

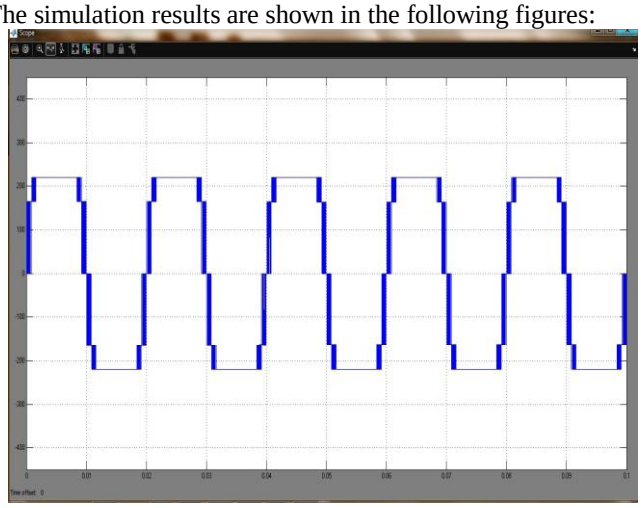

Fig 7. Output voltage of conventional CCMLI

As we can observe from figure (7) through figure (10), we get a better voltage waveform for H-bridge type flying capacitor multilevel inverter compared to conventional flying capacitor multilevel inverter. The THD for the modified inverter system is 26.98% as compared to 32 % for conventional capacitor clamped MLI.

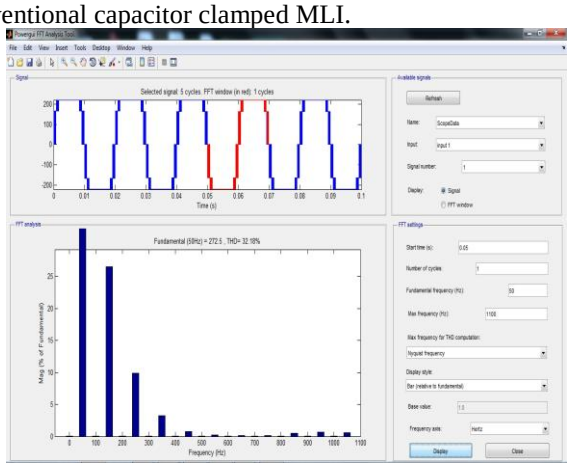

Fig 8. FFT-harmonic spectrum of output voltage of conventional CCMLI

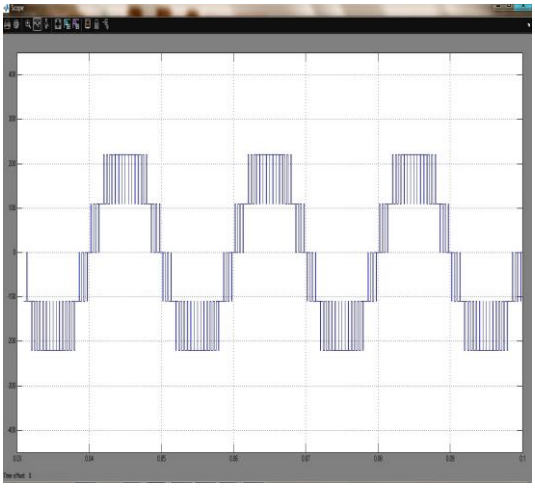

Fig 9. Output voltage of chosen H-bridge type CCMLI

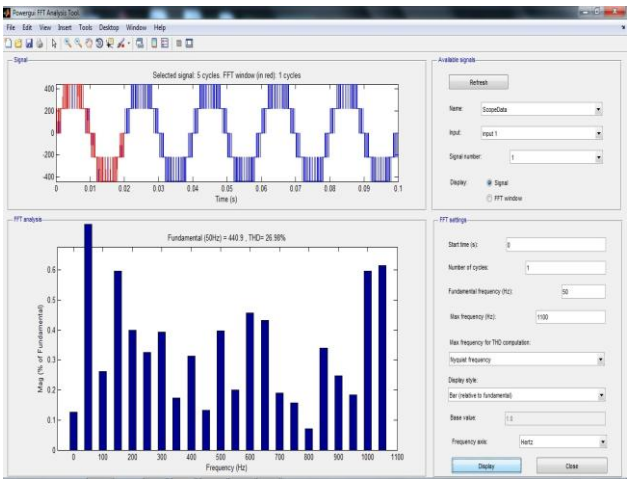

Fig 10. FFT-harmonic spectrum of output voltage of conventional CCMLI

V. FUTURE WORK

Using MATLAB Simulink tool, the closed loop control model of chosen CCMLI will be obtained. The control will be simulated using Proportional Integral Derivative(POD) controller. Using the controller values, a code will be developed which will be embedded in the dsPIC in the hardware implementation.

REFERENCES

[1] Malinowski, M., Gopakumar, K., Rodriguez, J., Pérez, M.A : "A survey on cascaded multilevel inverters", IEEE Trans. Ind. Electron., 2010, 57, (7), pp. 2197–2206

[2] McGrath, B.P., Holmes, D.G.: "Multicarrier PWM strategies for multilevel inverters", IEEE Trans. Ind. Electron., 2002, 49, (4), pp. 858–867

[3] Sneineh, A.A., Wang, M.-y., Tian, K.: "A new topology of capacitor-clamp cascade multilevel converters". Proc. IEEE 2006,Power Electronics and Motion Control Conf., August 2006, pp. 1–5

[4] Priyan, S.S., Ramani, K.: "Implementation of closed loop system for flying capacitor multilevel inverter with stand-alone photovoltaic input". Proc. IEEE 2013 Int. Conf. Power, Energy and Control (ICPEC), February 2013, pp. 281–286

[5] Maheshkumar.N., Maheskumar.V., Divya,.M.E.M.: "The new topology in flying capacitor multilevel inverter". Proc. IEEE 2013 Computer Communication and Informatics (ICCCI), January 2013, pp. 1–6

[6] Lai, J.-S., Peng, F.Z.: "Multilevel converters – a new breed of power converters". Proc. IEEE 1995 Industry Applications Conf., October 1995, pp. 2348–2356

[7] Palanivel, P., Dash, S.S.: "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques", IET Power Electron., 2011, 4, (8), pp. 951–958

[8] Ding, K., Cheng, K.W.E., Zou, Y.P.: "Analysis of an asymmetric modulation method for cascaded multilevel inverters", IET Power Electron., 2012, 5, (1), pp. 74–85