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# LEAKAGE POWER REDUCTION IN CMOS COMBINATIONAL CIRCUITS USING LECTOR TECHNIQUE

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***Abstract*— The shrinking of device size has led to use of lower supply voltage which in turn requires the lowering of threshold voltage. This has led to the increase in sub-threshold leakage current which results in increased power dissipation. In this paper we have utilized LECTOR technique to implement combinational circuits like NAND, NOR and EX-OR and then a comparative analysis of power and delay has been carried out. The simulation has been carried out on 180nm CMOS technology using Cadence Virtuoso tool.**

***Index Terms* — Deep Submicron, Sub-Threshold Leakage current, LECTOR, Transistor stacking, DTMOS.**

## I. INTRODUCTION

All Power consumption has been the bottleneck in achieving high performance. In deep submicron regime, as the device density is increasing, power consumption has emerged as a threat to the device reliability and signal integrity. Use of battery operated portable devices has paved the way to design of low power devices. Higher power dissipation leading to lower battery life, even in the idle mode, has resulted in quick and inventive growth of low power and high performance designs. The performance and the switching speed of MOS devices is controlled by the bias voltage (Vdd) and the threshold voltage (Vth). These controlling parameters scale down with the scaling down of technology node leading to increased power dissipation.

In digital CMOS circuits, power dissipation is categorized into three types-dynamic power dissipation, short circuit power dissipation and static power dissipation. Dynamic power dissipation also called as switching power dissipation is the largest contributor to the total power dissipation in CMOS circuits. Short circuit and static power dissipation contribute very less. But as the technology scales down, static or leakage power dissipation becomes prominent. The total power dissipation in a CMOS circuit is given as:

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{static} \quad (1)$$

In Eq. 1,

$$P_{dynamic} = C_L V_{dd}^2 f_{clk} \alpha$$

is the dynamic power dissipation. It mainly depends on switching activity ($\alpha$), power supply voltage ($V_{dd}$), load capacitance ($C_L$), and frequency ($f_{clk}$).

$$P_{short-circuit} = \frac{1}{12} k\tau f_{clk} (V_{dd} - 2V_{th})^3$$

is the short-circuit power dissipation resulting from the short circuit path between power supply and ground due to the simultaneously switching on of both p-type and n-type network of CMOS circuit. Here $\tau$ is the equal rise time and fall, time $V_{th}$ is the threshold voltage and *k* is the transconductance parameter.

$$P_{static} = P_{leakage} = V_{dd} I_{leakage}$$

is the static or leakage power dissipation where $I_{leakage}$ is the leakage current. With the increasing device density there is requirement for reduction of power supply voltage which ultimately leads to reduction in threshold voltage. This results in increase in sub-threshold leakage current, a dominant reason for increasing power dissipation and speed degradation.

There are three main sources of leakage current:[ 9]

1) Source/Drain leakage current
2) Gate direct tunneling leakage current
3) Sub-threshold leakage through the channel of an OFF transistor.

In this paper LECTOR technique is implemented for CMOS inverter and other combinational circuits like NAND, NOR and EX-OR. The power and delay analysis is done and the comparison is carried out. The results are shown in the tabular form.

## II. RELATED WORK

So far many techniques have been used for leakage power reduction each having their own merits and demerits. Some of the techniques are MTCMOS, DTMOS, Power Gating, Super Cutoff CMOS Circuit, Forced Transistor Stacking and Sleepy Stack. Most of the techniques aim at reducing the power by shutting down the power supply to the system or circuit during standby mode.

In transistor stack approach [4], the leakage current decreases when two or more series transistors are turned off. In sleepy stack approach [5], the first step of implementation is forced stacking and this followed by insertion of sleep transistor parallel to one of the stacked transistors. During active mode, the two parallel transistors are ON thereby effective resistance of the path is reduced resulting in reduced propagation delay. During standby mode, the sleep transistor is OFF and the stacked transistor reduces the leakage power.

In Dynamic Threshold CMOS (DTCMOS), the gate and body of each transistor are tied together. The leakage is low, when the transistor is OFF and the current will be high if the

transistor is ON.[6]. Multi threshold CMOS (MTCMOS) inserts extra transistor(s) either PMOS/NOMS or both called sleep transistor(s) into the design. During the normal mode of operation, these transistors set to "on" state without disturbing the functionality of the circuit. During the standby mode, these transistors switched to "off" state to isolate the power supply from the circuit. The isolated supply voltage causes the leakage currents to minimize[2]. Nevertheless, this technique increases the dynamic power dissipation of the circuit.

## III. LECTOR TECHNIQUE

The basic idea behind LECTOR approach is that "A state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path."[8][9].

### A. LECTOR based CMOS Inverter

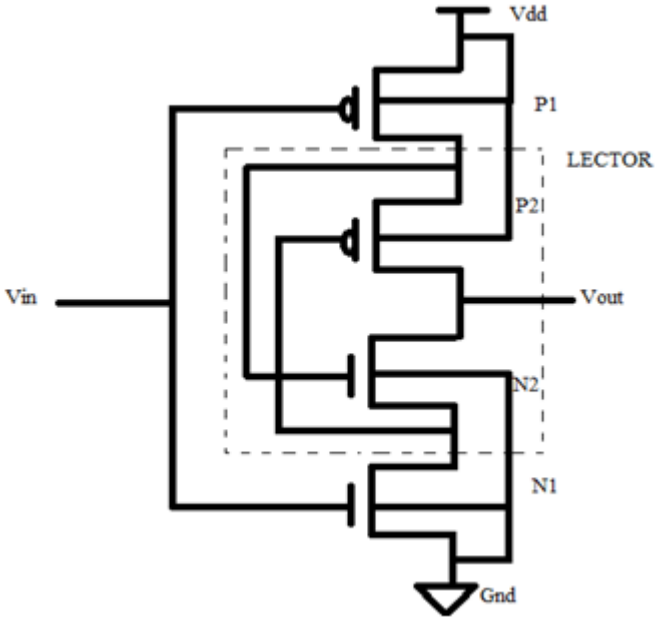


Figure 1: LECTOR CMOS Circuit

A p-type transistor and an n-type transistor connected in series form the LECTOR network as shown in Figure 1. This network is imported between the pull-up and pull-down network of the logic circuit. This way the Gate terminal of each Leakage Control Transistor (LCT) is controlled by the Source of the other thereby ensuring that one of the LCT's always operates in its near cut-off region.

In Figure 1 LECTOR based CMOS Inverter is shown. P2 and N2 are the leakage control transistors. Gate terminal of P2 is connected to the Source terminal of N2 and Gate terminal of N2 is connected to the Source terminal of P2. The Body terminal of all PMOS transistors are connected to the power supply voltage Vdd and the Body terminal of all NMOS transistors are connected to Ground (Gnd) terminal. When input Vin is LOW then N1 and P2 are OFF and when Vin is HIGH then N2 and P1 are OFF. This implies that the OFF resistance between the supply rails (Vdd and Gnd) is increasing and this causes reduction in leakage current

### A. LECTOR based NAND Gate

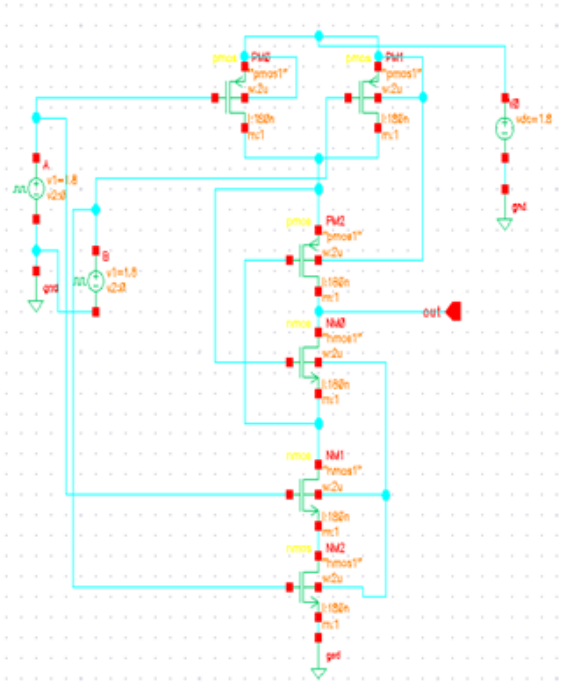

Figure 2: Schematic of Lector NAND Circuit

As can be seen in the Figure 2 above, between the pull-up and pull-down networks in a conventional CMOS circuits, Leakage Control Transistor network is inserted.

### B. LECTOR based NOR Gate

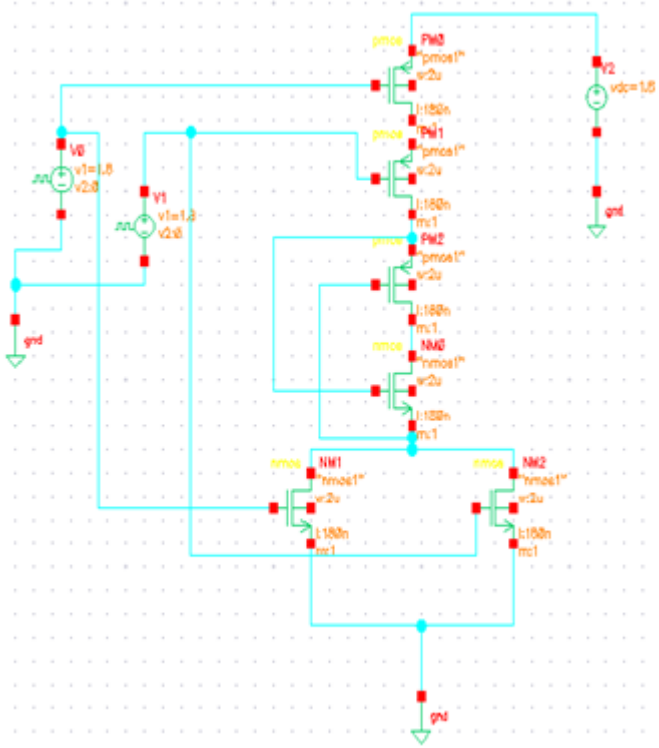

Figure 3: Schematic of LECTOR NOR Circuit

## IV. SIMULATIONS AND RESULTS

All the simulations is carried out using Cadence Virtuoso tool at 180nm technology. The supply voltage is 1.8V. The length and width of each transistor is 0.18µm and 2µm respectively.

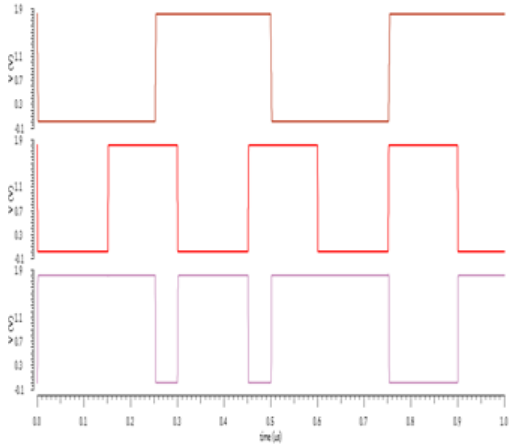

Figure 4: Simulation Result for LECTOR NAND

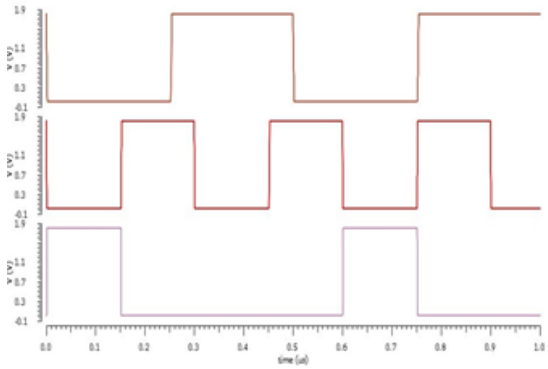

Figure 5: Simulation Result for LECTOR NOR

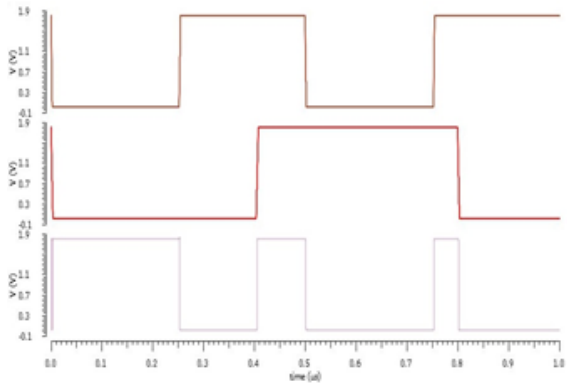

Figure 6: Simulation Result for LECTOR EX-NOR

TABLE 1. COMPARISON OF POPWER DISSIPATION FOR CMOS AND LECTOR CIRCUITS

| **Power Dissipation (µW)** | | |
|---|---|---|
| | ***CMOS*** | ***LECTOR*** |
| INVERTER | 1.32 | 0.444 |
| NAND | 1.78 | 0.516 |
| NOR | 1.68 | 0.426 |
| EX-NOR | 1.89 | 0.807 |

TABLE 2. COMPARISON OF PROPAGATION DELAY FOR CMOS AND LECTOR CIRCUITS

| | **Propagation Delay(ps)** | |
|---|---|---|
| | ***CMOS*** | ***LECTOR*** |
| INVERTER | 0.35 | 0.21 |
| NAND | 0.46 | 0.40 |
| NOR | 0.49 | 0.45 |
| EX-NOR | 0.63 | 0.196 |

## CONCLUSION

Using Cadence Virtuoso 180nm technology, INVERTER, NAND, NOR and EX-NOR circuits were simulated. The power dissipation and propagation delay were calculated and the comparison was done in tabular form. From the results obtained it can be verified that there is a significant amount of reduction in power dissipation of the circuits when LECTOR technique was used.

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