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DESIGN & OPTIMIZATION OF FINFET BASED DOMINO LOGIC CIRCUIT

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Abstract— **This paper presents a design technique of FinFET based AND gate using Domino Logic. Domino Logic offers smaller areas than conventional CMOS logic (Dynamic logic) and parasitic capacitances are smaller so that higher operating speeds are possible. In this paper we are designing 32nm DGFinFETs. A two – input AND gate is designed and simulated in 32nm technology using 32 nm double gates FinFET device. Simulation results indicate that the proposed technique provides improvement in noise tolerance of about four times and the use of FinFET device reduces the power consumption over the conventional MOSFET designs.**

Index terms- **FinFET, AND gate, Domino Logic, Power Consumption, ANTE, Noise Tolerance.**

I. INTRODUCTION

The Double-gate (DG) FinFET has been widely examined recently because of its performance potential, and excellent suppression of short-channel effects (SCE) and commensurate scalability, all stemming from the dynamic charge coupling between the two gates afforded by the ultrathin Si-fin body [1],and relatively easy fabrication and good integration features. Most recently, reports of fabrication of independent-gate FinFETs, with desirable characteristics such as dynamic threshold voltage (V_t) control and transconductance modulation, have been presented [2,3].

Such novel devices could relax requirements for gate work-function engineering for V_t control, and enable conventional MOS integrated circuits to be optimally designed with variable $–V_t$ devices. Unique among these devices are the multiple independent-gate FinFETs (MIGFET) [2], the technology for which also enables double gate FinFETs to be fabricated on the same chip. The scaling of conventional MOS transistor has been become increasingly difficult because of large short channel effects. Aggressive scaling of MOS device dimensions leads to lower noise tolerance and higher average power consumption [4].

Fin-type field effect transistors are the most promising substitute for bulk MOS at the nanoscale. This is because the fabrication technology of FinFETs is almost same as the conventional MOS transistor [5]. Domino logic circuit techniques are extensively applied in high-performance microprocessors due to super area and speed characteristics of dynamic CMOS circuits as compared to static CMOS circuits [6]. Dynamic MOS logic circuits are used in high performance VLSI chips achieves high performance of system. In design of dynamic logic circuits noise is a major issue. In deep submicron region the noise tolerance of dynamic logic circuit is very poor and they are prone to logic failure [7]. High-speed operation of domino logic circuits is primarily due to lower noise margins of domino circuits as it is compared to the static gates.

As on-chip noise becomes more with technology scaling and increasing operating frequencies, free of error operations of domino logic circuits has become a major challenge [8]. Figure 1 shows structure of multi-fin FinFET this device is consists of thin silicon body T_{si} is thickness, N is number of fins, h is height, p is fin pitch is the minimum pitch between adjacent fins allowed by lithography, p can be made as small as half of the lithography pitch.

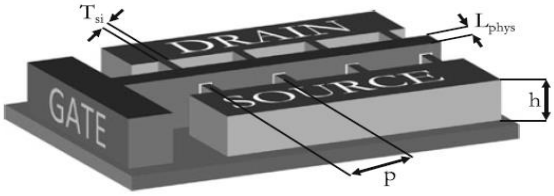


Fig. 1 Multi-fin FinFET

FinFET device is as follows In shorted-gate (SG) FinFETs, the two gates are connected together to a 3T device. This can serve as a direct replacement for the CMOS device. In independent-gate (IG) FinFETs top part of gate is etched out, giving way to two independent gates can be controlled separately. IG-mode has more design options as shown in Figure (2).

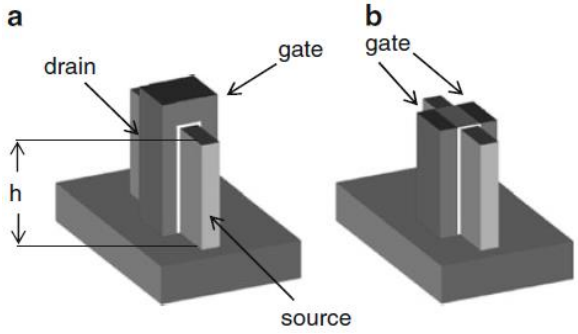


Fig. 2 (a) SG-mode FinFET (b) IG-mode FinFET

In standard domino logic gate a feedback keeper is employed to maintain the state of dynamic node against the coupling noise, and sub-threshold leakage current and charge sharing. The keeper transistor is turned on the beginning of evaluation phase. Provided that the necessary input combination to the discharge dynamic node is applied, the keeper and pull-down network transistors compete to determine the logical state of the dynamic node. This contention between the pull-down network and keeper transistors degrades the speed of the circuit while increasing the power consumption [6, 8]. The keeper transistor is typically sized smaller than that of the pull-down network transistors in order to minimize the delay and power penalty caused by a keeper contention current. A small keeper cannot provide necessary noise immunity for reliable operation in an increasingly noisy and noise sensitive on-chip environment in scaled conventional MOS technologies [6, 8]. There is a tradeoff between reliability and high-speed/energy-efficient operation in the domino logic circuits. New dynamic circuit techniques which can suppress the keeper contention current while maintaining high noise immunity are highly desirable.

In this paper, we propose a technique that this proposed technique has noise tolerant and has low power domino logic circuit and is designed using FinFET technology. We have designed a AND gate domino logic circuit which is simulated on HSPICE in 32 nm technology.

This paper is organized as follows: Section 1 gives brief introduction to the research work. Section 2 briefs about FinFET technology, includes literature survey and latest developments on FinFET technology. Section 3 and 4, describe two of the existing domino logic techniques in MOSFET that are implemented using FinFET technology. Proposed technique is described in Section 5. In Section 6, methodology and metrics used for analysis are presented and in section 7 and 8 simulations results and conclusions are presented.

II. FINFET TECHNOLOGY

FinFET Structure and Process Flow

A pictorial representation of a double-gate FET (DG-FET) is shown in Figure 1. The short channel effects in such a structure are well-controlled compared to single-gate devices due to control of the channel through two gates instead of one. The advantages of the Double Gate-FETs are the best realized when two gates are perfectly aligned with each other. The FinFET structure is one of a successful implementation of the double-gate device. Advantages in the electrical scalability and performance, it also provides benefits in fabrication and manufacturability. The layout and process flow are reasonably compatible with a existing bulk CMOS process, making it more attractive for the manufacturing [9]. Owing to it is superior fabrication and performance benefits, its production may start close to the 65nm technology node [10]. The issue of gate alignment and S/D alignment is very easily dealt with, in this implementation by rotating a silicon film of the planar double gate structure to a vertical orientation. Forming the gate around the fin now makes the gates self-aligned along with self-alignment of the S/D regions.

In this section architecture of device for independent-gate and tied-gate FinFETs are offered. P-type and N-type FinFETs with 32nm (nanometer) channel length are characterized and designed using MEDICI, it is a physics based device simulator [11].

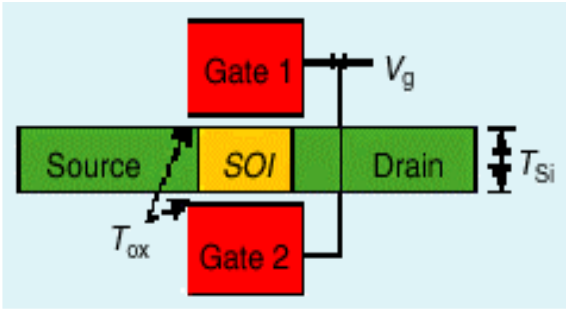


Fig 3. Double gate MOSFET

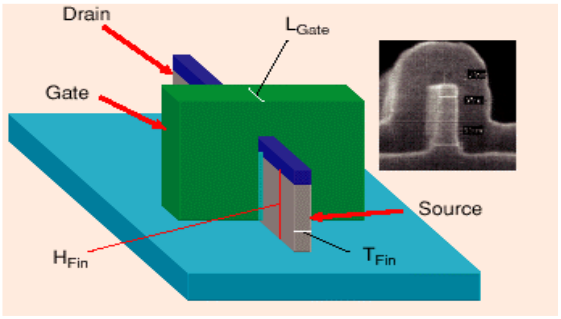


Fig 4. FinFET Structure.

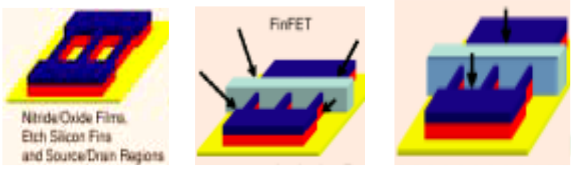


Fig 5. FinFET manufacturing process flow

The three dimensional architectures of the independent-gate and the tied-gate FinFETs are shown in Fig. 6. A top view of a FinFET indicates the critical physical dimensions are shown in Fig. 6c. In this paper FinFETs technology parameters are listed in Table 1 [12]. The width of FinFET is quantized due to a vertical gate structure. The H_{fin} (fin height) it determines the minimum transistor width (W_{min}). With the two gates of a single-FinFET tied together, W_{min} is:

$$W_{min} = 2 \times H_{fin} + t_{si}, \quad (1)$$

Where t_{si} is the thickness of the silicon body and H_{fin} is the height of the fin as shown in Fig. 1. The fin thickness is much smaller than fin height in order to effectively prevent the

dissemination of the short-channel effects and to enhance the efficiency of area in a double-gate FinFET [13].

Table 1
Device technology parameters.

Parameter	Value
Channel length (L)	32 nm
Effective channel length (Leff)	25.6 nm
Fin thickness (tsi)	8 nm
Fin height (Hfin)	32 nm
Oxide thickness (tox)	1.6 nm
Channel doping	10^{15} cm^{-3}
Source/drain doping (N-type and P-type FinFETs)	2×10^{20} cm^{-3}
Gates work function (N-type FinFET)	4.5 eV
Gates work function (P-type FinFET)	4.9 eV
Supply voltage (VDD)	0.8 V

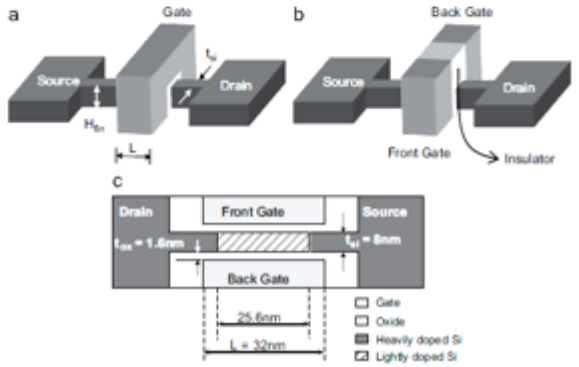


Fig 6. The device architectures of FinFETs. (a) 3D structure of a one-fin tied-gate FinFET. (b) 3D structure of a one-fin independent-gate FinFET. (c) Cross-sectional top view of a FinFET with a drawn channel length of 32 nm.

Therefore H_{fin} is the dominant component of the transistor width. Since H_{fin} and t_{si} are fixed in FinFET technology, to increase the width of a FinFET multiple parallel fins are utilized as it is shown in Fig. 6.

$$Wtotal = n \times Wmin = n \times (2 \times Hfin + tsi). \quad (2)$$

The two vertical gate sofa single – FinFET can be separated by an oxide on the silicon fin top, thus forming an independent gate FinFET as shown in Fig. 6b. An independent – gate FinFET provides two different active modes of operation with different current characteristics determined by independent bias conditions of two gates as it is shown in Fig. 8. In dual-gate mode to control the development of a channel two gates are biased with the same signal.

On the other hand, in the single gate mode one of the gates is biased with input signal to induce the inversion of channel although the other gate is disabled. The two gates are coupled strongly in the dual gate mode, thereby lowering the threshold voltage $|V_{th}|$ as it is compared to single gate mode. For example in the dual gate mode is 2.77 times higher the maximum drain current formed as compared to single gate mode in a minimum sized P-channel FinFET as it is shown in Fig. 8. FinFET switched gate capacitance is also halved in the single-gate-mode.

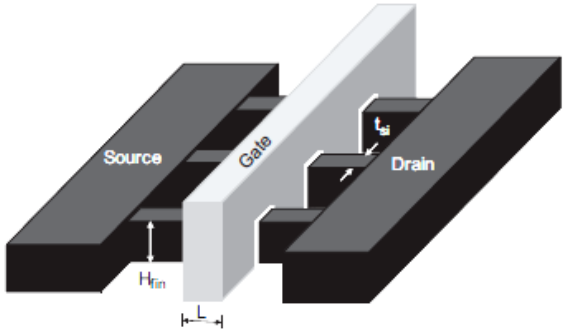


Fig 7. Three – FinFET. $W_{total} = 3 \times (2 \times H_{fin} + t_{si})$.

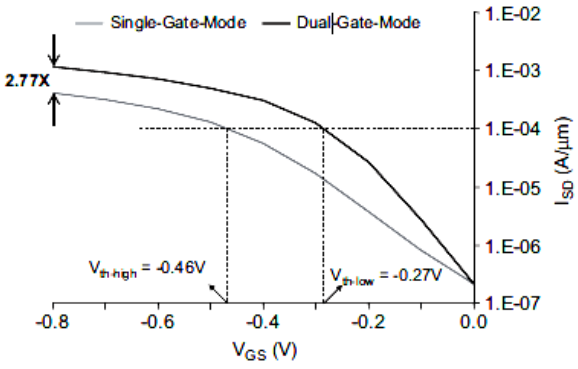


Fig. 8. Drain current characteristics of a single-fin P-type IG-FinFET. The source-to- drain voltage is 0.8V. T = 110 1C. I off = 216nA/mm. Ion (single-gate-mode) = 0.422 mA/um. Ion (dual-gate-mode) = 1.17mA/um. The threshold voltage is the gate-to- source voltage at which the drain current per fin height is10^{-4} A/um for |VDS| = VDD.

A. Domino Logic Circuits

Performance critical paths in the high-performance integrated circuits are often implemented with the domino logic circuits [6, 8]. Although domino logic circuits are preferable in the high-speed applications, the reliability of the domino logic circuits is seriously degraded with the technology scaling. The operating principles of the domino logic circuits are reviewed in this subdivision. The speed versus noise immunity and power tradeoffs in the standard domino logic circuits. Thus, new variable threshold voltage independent-gate of FinFET keeper technique, simultaneously intensify the evaluation speed and lowering power consumption in the FinFET domino logic circuits [12].

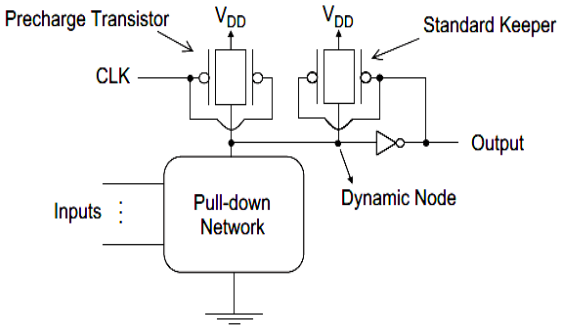


Fig. 9. A standard footless domino circuit in a tied-gate FinFET technology.

III. DOMINO LOGIC AND GATE WITH INDEPENDENT GATE (IG) TECHNIQUE USING FINFET

Figure 10, shows the schematic of a two input domino AND gate using FinFET technology.

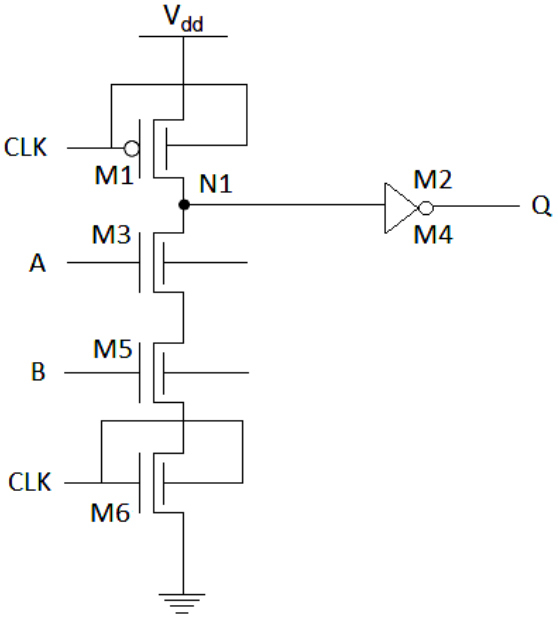


Fig. 10. Domino AND Independent Gate using FinFET.

The Domino logic circuits are preferable in the high speed application. The reliability of the domino logic circuit is seriously degraded with the technology scaling. The operating principles of the domino logic circuits are derived in this subdivision. Under two phases the domino logic circuit works namely, precharge phase and evaluation phase. When clock is zero (CLK = 0) & it is called precharge phase the internal node N1 is precharged to V_{dd} as M1 is on and M4 off to VDD as M1 is on and M4 off is disabled pull down. Basically it means ground has no path when clock (CLK) is = 1 it is called Evaluation phase M1 is off and M4 is ON.

According to the inputs, the outputs can be evaluated. The two gates are can be evaluated the gates are tied together in the schematic order to form independent gate (IG) the inverter at the output gives the standard domino logic functionality. There If clock (CLK) goes high in domino logic circuit once the output has been discharged it will not go high again until the next cycle of clock (CLK).

IV. TWIN TRANSISTOR AND INDEPENDENT GATE (IG) TECHNIQUE USING FINFET

The twin transistor device features the low-voltage, low current operation required in portable, battery – powered applications and its miniature 6 – pin package makes it ideal for size – constrained designs like Cellular Phones, Cordless Phones, iPhone Tablets, ipads, Laptops, Bluetooth speakers, Pagers, iPods, Mp3 players and PCMCIA cords. For the improvement in the noise tolerance of the Domino logic circuits, many techniques have been previously introduced using (Metal Oxide Semiconductor field effect transistor (MOSFET) like Twin Transistor Technique. In this research paper we have implemented the twin transistor technique using FinFET device in independent gate configuration.

In figure 11, shows the twin transistor technique Schematic using FinFET technology.

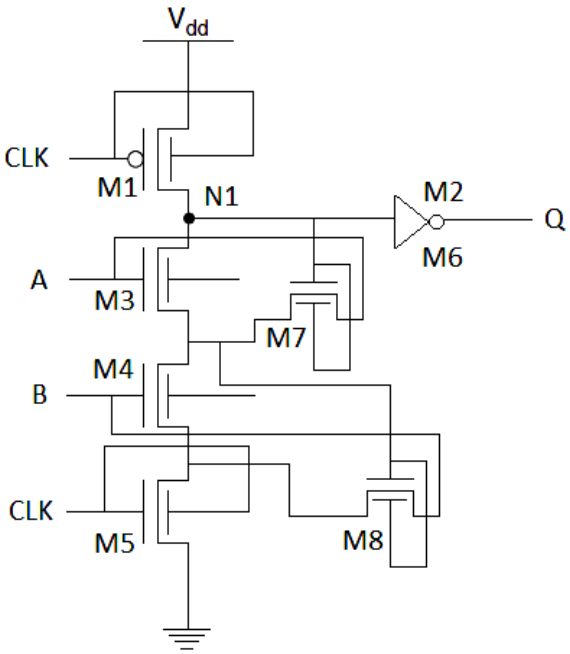


Fig 11. Twin Transistor AND Independent Gate using FinFET.

In this technique, two transistors M7 and M8 are named as twin transistors are added in the Domino logic circuit. The purpose of adding twin transistors is to increase the turn on voltage that is threshold voltage of the pull down network (PDN). As in the above independent gates M2 and M3, therefore both the gates have been given direct current (D/C) voltage on 0.7 volts and V_{dd} as DC = 1.0 volt. This is done by pulling up the voltage of source node of transistor M2 and M3.

V. PROPOSED TECHNIQUE

Figure 12 shows the schematic diagram of our proposed technique. For better noise tolerance ANTE using FinFET. The proposed technique has two additional transistors added to increase the noise tolerance of AND gate IG. The two additional transistors one M2, M5, M6 are shorted gates where as in this schematic diagram two transistors. M3 and M4 is independent gate. The transistors used in the above figure are explained as follows:-

In the circuit two clock signals are used in the technique that is CLK and DCLK (Delay Clock). By delaying the CLK (clock) signal delayed clock consist of series of inverters.

In increasing the noise tolerance of the AND gate a delayed clock signal is fed to M5 transistor.

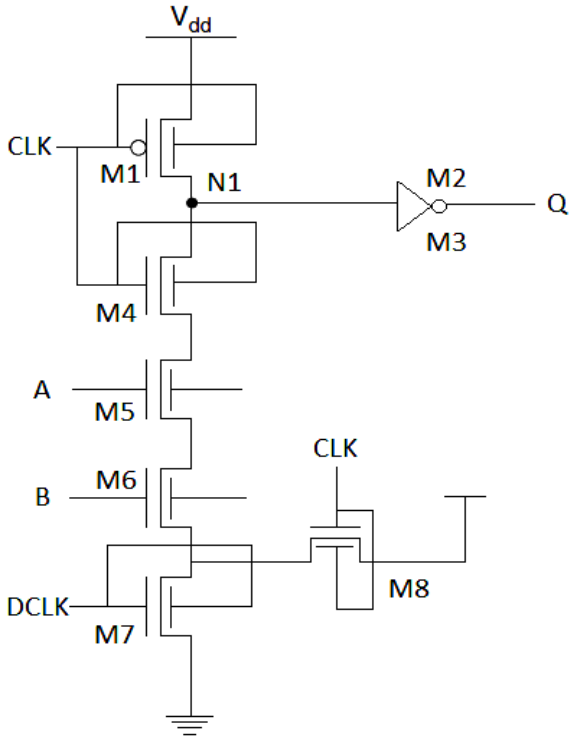


Fig 12: Proposed Technique AND Independent Gate using FinFET.

A. Improved Noise Tolerance Process of Proposed Technique

The Noise tolerance of the proposed technique is improved by:-

M2 as Stacking Transistor: When clock is zero (CLK=0), m1 IS on and m2 is off and the node n1 is precharged to Vdd. There is no leakage path to ground as transistor M2 is off. In this proposed technique it reduces the leakage noise. Change sharing is also reduced as the path to pull down Network (PDN), remain closed. This stacking effect improves the noise tolerance.

Raising Source Voltage of PDN: - By raising the source voltage of pull down network the threshold voltage of the pull down network is improved. As shown in figure 12. The transistor M6 is added to increase the common source voltage of the pull down network (PDN). This causes the source body biasing voltage to increase, this resulting in the increase of the threshold voltage of the n- type FinFET in pull down Network (PDN), this it can now tolerable more amount of noise at its inputs.

Delayed Clock (DCK):- In the figure 12 proposed techniques the transistor M5 is fed with a delayed clock signal (DCLK). In the evaluation phase of clock is 1(CLK=1), M1 is off and M3 is ON. The output is evaluated to its inputs. As the delayed clock is still low, the transistor M6 is off. In this the path between node N1 and ground is shut down. Then, leakage noise is reduced further and therefore in this proposed technique the noise immunity is improved.

VI. METHODOLOGY

The Domino Logic Technique FinFET, Twin Transistor technique FinFET and the proposed technique is simulated on HSPICE Software tool. The model used for FinFET circuit analysis is BSIMIMG for 32nm FinFET device.

BSIM-IMG is a model for MG transistors which is implemented in Verilog –A. This model describes all the important behavior of MG transistor. It is physics based model which is scalable and predictive over a wide range of device parameters BSIM-IMG, Independent Multi-Gate model, has been developed to model the electrical characteristics of the independent double-gate structures like Ultra-Thin Body and BOX SOI transistors (UTBB). It allows different front- and back-gate voltages, work functions, dielectric thicknesses, and dielectric constants [14].

To quantify the noise immunity and performance of the techniques, certain metrics are considered. The parameters used for comparison are Average Power Consumption, Average Noise Threshold Energy (ANTE) and Delay. The proposed technique is compared with Domino FinFET and Twin transistor FinFET techniques. A comparative study of proposed technique using FINFET and MOSFET is also analyzed on the basis of average power consumption.

The metrics considered for comparative analysis are :

A. Average Noise Threshold Energy

The Average Noise Threshold Energy (ANTE) metric is defined as the average input noise energy that the circuit can tolerate. The ANTE metric is defined as

ANTE= E (An^2.Wn)

Where An and Wn are the amplitude and width of the input noise pulse, respectively, and E ( ) is their average. To obtain the ANTE of a dynamic circuit, it is necessary first to get its noise immunity curve.

B. Average Power Consumption

The power consumed by device logic from one state to another. It denotes the power consumed by any circuit for its functioning properly. The unit of power is in Pico Watt (pW).

Therefore it is the power consumed by circuit. For low power devices this parameter should be low.

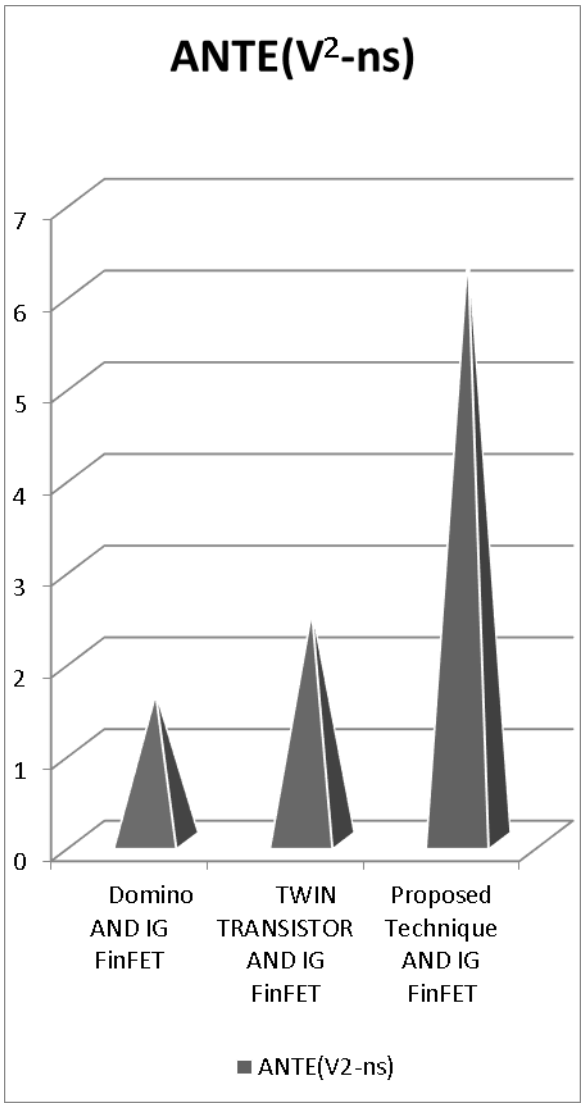
C. Delay

The delay of the circuits under test is measured as the difference in time between 50% points of raising the clock edge and falling dynamic node, assuming that the input signal has been set early enough relative to the rising edge of the clock signal.

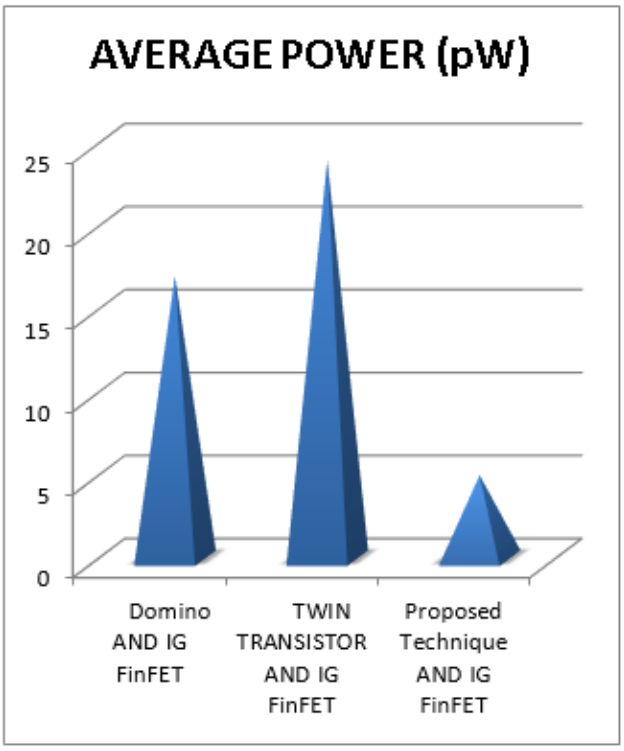
VII. STIMULATION RESULTS

In this section, we present the results of HSPICE simulation using the FinFET at 32 nm technology. The comparison between Domino technique, twin transistor technique and proposed technique are presented in graph 1, 2 and 3. The stimulation is carried out with 1.0 volt. Supply voltage and 27 ^{o}C temperature and 1.6 nm FinFET diameter. The metrics for comparison are average power consumption, delay and average noise threshold energy (ANTE). The graphs for comparison between the three above mentioned techniques are presented in the figures.

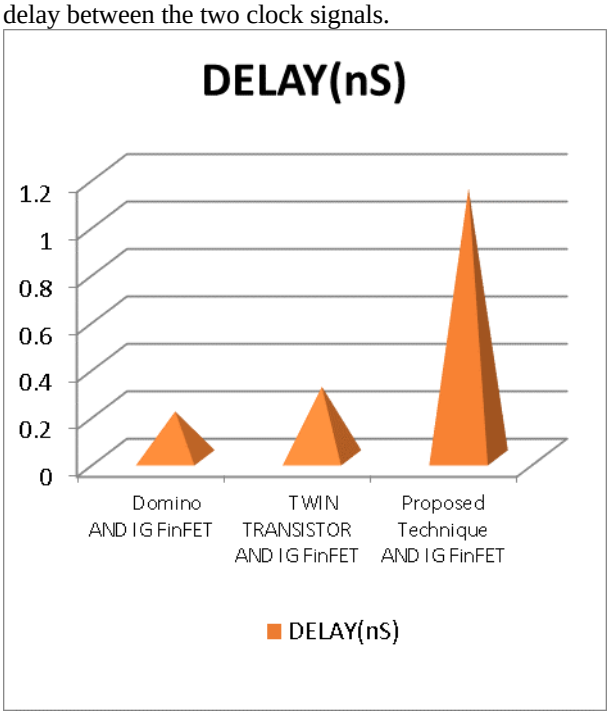
The chart in graph 1 shows that the Average Noise Threshold Energy (ANTE) of the proposed technique is showing the best result among all the techniques. The ANTE of proposed technique about 4.5 times better than that of domino technique and 2.3 times better than twin transistor technique FinFET.



The charts shown in graph 2 shows that the average power consumption in this technique. It indicates that the average power consumption is least in proposed techniques. Where as in domino technique the average power consumption is low as it is compared to twin transistor techniques. Thus we can say that the power consumption is high in twin transistor technique as it is compared with the other two techniques.



Graph 3, Shows delay in the techniques. As the path of the signal is same the delay domino technique and twin transistor technique is almost same. There is an increase in delay in the proposed technique because when we used independent gate the delay becomes high. This can be adjusted by reducing the delay between the two clock signals.



METRIC/ TECHNIQUE	DOMINO AND IG FinFET	TWIN AND IG FinFET	PROPOSED AND IG FinFET
ANTE (V^2-nS)	1.6	2.5	6.4
AVERAGE POWER (pW)	17	24	5
DELAY (nS)	0.196	0.300	1.136

Table 1:- Performance comparison for 2 – Input AND Domino Independent Logic Gate.

VIII. CONCLUSIONS

The use of FinFET in the proposed technique reduces average power consumption. It indicates that FinFET is a promising device beyond 32nm technology. The reduced short channel effects in FinFET and better control over the gate of the FinFET improves the average power consumption in the designed techniques. As already shown in simulation results, the proposed technique has highest noise immunity, but this is achieved at the cost of higher delay in the proposed technique.

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