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A SURVEY PAPER ON DESIGN OF SRAM FOR WEARABLE ELECTRONICS

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Abstract: **In modern trends, the demand for memory has been increases tremendously. Also it is well known that in low scale technology reliability and variations average power consumption are the main design challenges. As Static Random Access Memory (SRAM) is used in high speed applications such as cache memory and occupies about 90% of silicon area various research works have been done to trim down its power consumption. This paper represents the issues in nanoscale memory design, which will have a ubiquitous presence in commercial electronic market.**

Keywords—**SRAM, low scale technology, reliability, average power consumption.**

I INTRODUCTION

SRAMS IN WEARABLE ELECTRONICS

In today's world, microcontrollers (MCUs) are found in a wide array of devices. The growing market of portable electronics devices demands lesser power dissipation for longer battery life and compact system. A major electronics boom that we're experiencing today is in wearable electronics (figure1).

Figure 1: Requirements of wearable electronics is driving the resurgence of SRAMs.

For wearable such as smart watches and health bands, size and power are critical factors. Due to limited board size, the MCU has to be very small and able to run on the frugal power provided by portable batteries.

To fulfil the above requirements, on-chip cache is limited. In future generations, we can expect more functionality to be associated with wearable. In such a case, the on-chip cache will fall short and the need will arise for an external cache. Of all the memory options available, SRAMs would be the most fitting option to act as an external cache. This arises from their lower standby current consumption compared to DRAM, and lower access time than both DRAM and Flash.

However, to fit into the tiny wearable boards, SRAMs will need to evolve. Between then and now, processors have become more powerful and have shrunk in size [1].The problems with existing parallel SRAMs include:

- Too many pins required for communicating with the MCU
- Too large to fit on the PCB.
- Increased susceptibility to soft errors: Soft error rates are expected to increase seven-fold [2] as process technology scales from 130nm to 22nm.

The Internet of Things and SRAMs

For the last few decades, the SRAM space has been divided between two distinct product families – fast and low-power, each with its own set of features, applications, and price. The devices where SRAMs are used need it for either its high-speed or its low power consumption, but not both. However, there is an increasing demand for high-

performance devices with low power consumption to perform complex operations while running on portable power. This demand is driven by a new generation of medical devices, handheld devices, consumer electronics products, communication systems, and industrial controllers, all driven by the Internet of Things (IoT).

The growth of IoT is headed in two distinct directions – smart wearable and automation. Wearable, as we discussed earlier, will be serviced best by SRAMs that have a small footprint and low power consumption. At the same time, the impact of the Internet of Things will be felt in industrial, commercial, and large-scale operations, and for automating individual houses to vast factories and entire cities. SRAMs that can retain high-speed performance while reducing power consumption in a small package will offer significant value in IoT applications.

Thus, to be a preferred choice for IoT designs, SRAMs will have to evolve in such a way that a customer needs not worry about a trade-off between performance and power.

The key areas of innovation for SRAMs include

- *Smaller sized chips:* This calls for advancement in process technology as well as innovation in packaging
- *Lower pin count:* Currently, most SRAMs have parallel interface. Serial SRAMs in the market have only low density options. The need would be to manufacture higher density Serial SRAMs
- High performance chips that consume less power
- On-chip soft-error correction.

II INNOVATION IN THE DESIGN OF SRAM

The small size of the transistors causes an increase in leakage current [3] which in turn increases the standby power consumption. In the following sections, here describe some of the key innovations in the design of SRAMs that are driving embedded developers to consider their use in their embedded wearable, IoT, and other embedded systems applications.

A Chip Scale Packaging

Chip scale packaging (CSP) [4] is a powerful technique to reduce the size of chips. As per specifications (J-STD-012), to qualify as 'chip scale' the overall packaged part must have an area not more than 1.5 times that of the die and a linear dimension not more than 1.2 times that of the die. In contrast, for a standard packaged die, the overall chip area could be as high as ten times that of the die. Thus chip scale packaging can help reduce the size of a chip manifold. A similar size reduction could be achieved by shrinking the process node. However, in the case of SRAMs, migrating to a smaller process node is fraught with risks, as already explained.

This reduction in area is achievable by eliminating the first level packaging – lead frame, die attach, wire bonds, and mould compound. CSP chips are mostly packaged at the wafer level where the packaging material is deposited directly on the wafer. The pinout is similar to BGA (ball grid array packaging) whereby solder bumps on the package act as pins. A similar size reduction could be achieved by shrinking the process node.

A CSP SRAM would definitely be an excellent fit for space-constrained boards in wearable applications. It is much easier to design-in than the next best alternative: buying an SRAM die and packaging it along with the MCU die using sophisticated MCP (multi-chip packaging) techniques. Currently, CSP SRAMs are not in mass production (some suppliers offer it as a made-to-order option), possibly because the target market (wearable) has yet to move beyond the embedded niche. However, most of the key players in the SRAM market offer a CSP option for many of their other products. Cypress Semiconductor, for example, has CSP versions already available for its product families such as PSoC. Thus, it should not be difficult for manufacturers to extend the same capability to SRAMs.

B Lower Pin Count

While SRAMs consume less power than Flash and DRAM, a key problem of using SRAMs for memory expansion is its parallel interface. While a parallel interface allows faster read-write times, too many IOs are required for interfacing. For example, consider interfacing a 1Mb SRAM (64Kb x16) with an MCU. The number of IOs required would be 32 (16 address, 16 data). Multiplexing could bring that down to 24. But with every subsequent increase in density (2M, 4M, 8M etc.), the number of pins increases by 1.

The number of IOs available to interface with SRAMs in a tiny wearable board is limited because small MCUs have low pin count packaging. To connect with these MCUs,

SRAMs will have to move beyond the traditional parallel interface. The success of Serial Flash, EEPROM, etc. reinforce the market's need for a serial memory option. Since MCUs having been using embedded cache for years, the need for serial SRAM has not been felt until recent years. Serial SRAMs make interfacing simpler and less pin consuming (two for single SPI, two for dual SPI, and four for quad SPI). In addition, the number of IOs required does not increase with density.

As of today we have serial SRAMs in low density and comparatively lower access speed (up to 25ns access time and 1M density). In the near future, we can expect improvements in both these parameters. As the wearable products enter subsequent generations, we can expect that MCUs will be required to perform more complex operations. In such cases, it would be useful to have a higher density cache/scratchpad memory with higher throughput. Thus the evolution of serial SRAMs towards higher speed and density will be useful for the market. A size reduction using CSP packaging coupled with serial interface will make SRAMs a powerful option for both cache and scratchpad memory in wearable.

C High Performance with Low Power

Today there are two distinct families of asynchronous SRAMs: fast SRAMs (with high access speed) and low-power SRAMs (low power consumption). From a technological standpoint, this trade-off is justifiable. In low-power SRAMs, special GIDL (gate-induced drain leakage) control techniques are employed to control standby current and thus standby power consumption. These techniques involve adding extra transistors in the pull-up or pull-down path as a result of access delay increases, and in the process, increases access time. In fast SRAMs where access time is the priority, such techniques cannot be used. Moreover, to reduce propagation delay, die size is increased. This increase in die size increases leakage and, in the process, the overall standby power consumption.

So far this trade-off was acceptable by typical SRAM applications: Battery-backed applications used Low-power SRAMs (compromising performance) while wired industrial high-performance applications used fast SRAMs. However, for IoT applications and many other advanced applications such a trade-off will not serve well. The main reason is that for most of these applications, high performance is important while standby power consumption has to be limited as well, since most of these applications will be operating on battery power. Fortunately, SRAMs are evolving to bridge the performance gap between these two families towards a single chip with the benefits of both.

Microcontrollers long ago introduced the deep-sleep mode of operation. This mode of operation helps in power savings for applications that are in stand-by state most of the time. The controller can run at full speed during normal operation but goes into a low-power mode afterwards, thereby saving power. It is important that a similar operation is available for interfaced SRAMs too. Asynchronous Fast SRAMs with a deep-sleep mode of operation [5] make it an ideal choice for such applications. These SRAM chips have an additional input pin that helps the user toggle between different modes of operation (normal, standby, and deep-sleep). Thus, effective power consumption can be managed without compromising performance.

D On Chip Error Correction Capabilities

As memory process technology scales for improved performance and power, reduced voltage and shrinking node capacitance makes these devices more susceptible to soft errors. Today, CMOS technology has shrunk to such a size that extra-terrestrial radiation as well as chip packaging cause failures at an increasing rate. Traditionally, soft errors have been dealt with through the use of ECC (error correcting code) software or through redundancy (i.e., multiple SRAMs storing the same data), especially in systems where reliability is of paramount importance, such as medical, automotive, and military systems. However, this is expensive and requires extra board space.

Major SRAM manufacturers have started implementing error correction features directly on-chip [6]. To limit the effects of soft errors on modern semiconductor memories at a chip level, two architectural enhancements are used: on-chip ECC and bit interleaving. Through on-chip ECC, the software to implement error detection and correction of single-bit errors is hard-coded into the SRAM. Some

manufacturers even offer the option of an extra error pin to indicate the detection and correction of single-bit errors.

Bit interleaving, on the other hand, is used to limit the effect of multi-bit errors (i.e., a single energetic particle flipping multiple bits). Bit interleaving works by arranging adjacent bit lines to different word registers. This converts a multi-bit error into multiple single-bit errors, which can then be corrected by the on-chip ECC.

III SRAMs AND THE FUTURE

Low power LSI technology is becoming an increasingly important and growing area of electronics. In particular, low power RAM is a major area of this technology in which there has been rapid and remarkable progress in power reduction, with strong potential for future improvements. In large memory capacity RAM chips, active power reduction is vital to realizing low-cost, high reliability chips because it allows plastic packaging, low operating current, and low-junction temperature. Excessive power dissipation increases temperature and with every 10^0C increase in operating temperature, approximately doubles a component's failure rate[10].

As the low power design is a growing class of personal computing devices, such as portable electronics and communication devices. These devices and systems require high speed, complex functionalities and real time processing, capabilities [11]

Due to these problems; circuit designers are realizing the importance of limiting power consumption at all levels of the design. Scaling of CMOS devices has provided remarkable improvement in performance of electronic circuits in the past few years. But this scaling causes leakage in the circuit.

IV CONCLUSION

This paper focuses on the key innovation in the design of SRAM as the trend of SRAM technology is moving towards high-density, high-speed and low-power. Higher density and higher speed are achieved by scaling. Reduction of the gate oxide leakage current is essential to achieve high-speed keeping low standby current. Pattern formation processes, lithography and dry etching are the main concerns to miniaturization [7]

Exciting times are ahead for SRAM technology. The technological trends and advancements favour a grand comeback for this technology, whose adoption has been declining for years. ECC-enabled chips are already in production. Fast SRAMs with on-chip power management are also available. Serial SRAMs are in production but mostly for very low density applications and so are currently not comparable in speed to parallel counterparts. None of the traditional SRAM companies have launched serial SRAMs yet.

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