International Journal of Technical Research and Applications e-ISSN: 2320-8163,
www.ijtra.com Volume 5, Issue 4, (July-August) 2017), PP. 01-06

SIMULATION, DESIGN AND CONTROL OF A MODIFIED H-BRIDGE SINGLE PHASE SEVEN LEVEL INVERTER

[1]Atulkumar Verma, [2] Prof. Mrs. Preeti Khatri
[2] Assistant Professor
[1] pursuing M.E. Electrical Power Systems in PVG's College of Engineering & Technology,
Savitribai Phule Pune University, Pune – 09
[2] Assistant Professor in PVG's College of Engineering & Technology,
M.E. guide and pursuing PhD in Savitribai Phule Pune University, Pune – 09
[1] mehta.hrishi@gmail.com, [2] atul.ss.verma40@gmail.com,[3] khatri_preeti@yahoo.co.in

Abstract— Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. These inverters promise a lot of advantages over conventional inverters especially for high power applications. Some of the advantages are that the output waveforms were improved since multilevel inverter produced nearly sinusoidal output voltage waveforms. Hence the total harmonic distortion is also low. The switching losses also become less. And, the filter needed to smooth the output voltage is small; hence, the system is compact, lighter and much cheaper. In this paper, a modified single phase seven level inverter is simulated using MATLAB Simulink. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels (Vdc, 2Vdc/3, Vdc/3, 0, -Vdc, -2Vdc/3, -Vdc/3) from the dc supply voltage.

Keywords— Seven Level Inverter, pulsewidth-modulated (PWM), total harmonic distortion (THD).

I. INTRODUCTION

HE concept of multilevel inverters, introduced about 20 years ago, entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. Considering these advantages, multilevel converters have been gaining considerable popularity in recent years [1]. The benefits are especially clear for medium-voltage drives in industrial applications. In fact, several IEEE conferences now hold entire sessions on multilevel power conversion.

Several topologies for multilevel inverters have been proposed over the years; the most popular being the diode-clamped, flying capacitor and cascaded H-bridge structures [2]. Diode-clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. However, balancing of the capacitors is very complicated especially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems.

One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different dc voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters. Past research has shown this concept for cascading two-level inverters and multilevel inverters [3]. An advantage of this approach is that isolated sources are not required for each phase. One advantage is that cascaded inverters provide a compounding of voltage levels leading to extremely low harmonics. Another advantage is that the bulk inverter may be commercial-off-the-shelf; requiring hat only the lower-power condition inverter to be custom made. Yet another advantage is that the cascaded design avoids a large number of isolated voltage sources which would be cumbersome in grid connected power systems. An additional advantage is that the dual inverter structure may be useful for redundancy providing remedial operation for survivability [4-6]. However this topology requires separate DC voltage sources for each cascade. It therefore becomes difficult to control this topology in multilevel inverters as the number of levels goes up.

This paper proposes a modified H-bridge single phase multilevel inverter topology which combines the advantages of both diode-clamped inverters and cascaded H-bridge inverters. Moreover this new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. The reduced harmonic distortion is achieved for a new topology of multilevel inverters using sine PWM technique. The inverter scheme is simulated in MATLAB Simulink environment. The simulation results are presented to demonstrate the effectiveness of the proposed control. Section II describes the inverter topology and its operation. Section III discusses PWM modulation that is used for this model. Simulation and its results are included in Section IV and section V concludes the paper.

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed single-phase seven-level inverter was developed from the five-level inverter in [7]–[11]. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C1, C2, and C3, as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. The power generated by the

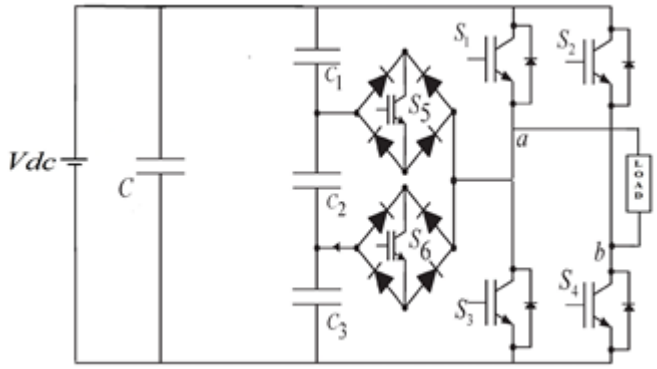


Fig. 1. Proposed single-phase seven-level inverter with modified H-bridge topology

inverter is delivered to a R or R-L load. Proper switching of the inverter can produce seven output-voltage levels (Vdc, 2Vdc/3, Vdc/3, 0,−Vdc,−2Vdc/3,−Vdc/3) from the dc supply voltage [12].

The proposed inverter's operation can be divided into seven switching states, as shown in Fig. 2(a)–(g). Fig. 2(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage.

The required seven levels of output voltage were generated as follows.

1) Maximum positive output (Vdc): S1 is ON, connecting the load positive terminal to Vdc, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc. Fig. 2(a) shows the current paths that are active at this stage.

2) Two-third positive output (2Vdc/3): The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 2Vdc/3. Fig. 2(b) shows the current paths that are active at this stage.

3) One-third positive output (Vdc/3): The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/3. Fig. 2(c) shows the current paths that are active at this stage.

4) Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 and S2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.

5) One-third negative output (−Vdc/3): The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to Vdc. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{ed}$ /3. Fig. 2(e) shows the current paths that are active at this stage.

6) Two-third negative output (−2Vdc/3): The bidirectional switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −2Vdc/3. Fig. 2(f) shows the current paths that are active at this stage.

7) Maximum negative output ($-V_{dc}$): S2 is ON, connecting the load negative terminal to V_{dc}, and S3 is ON, connecting the load positive terminal to ground. All

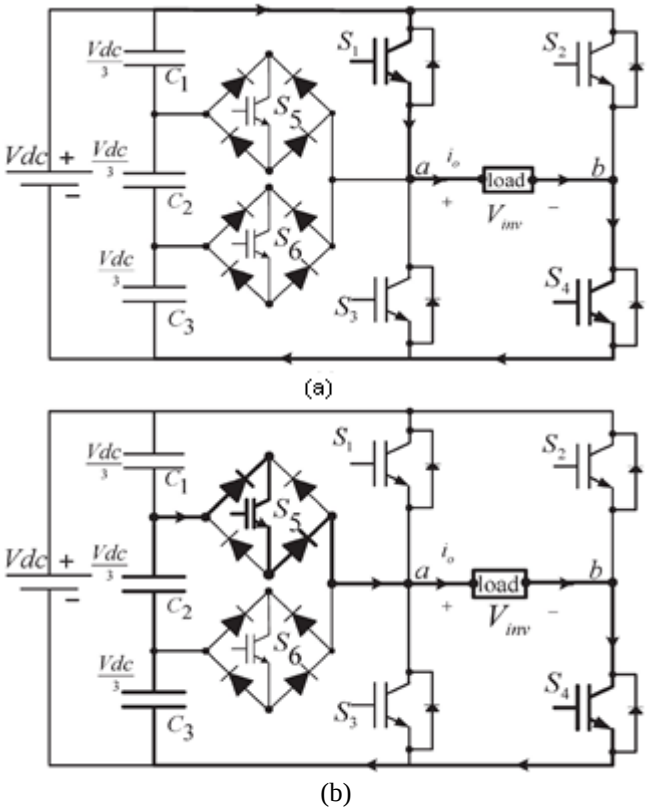
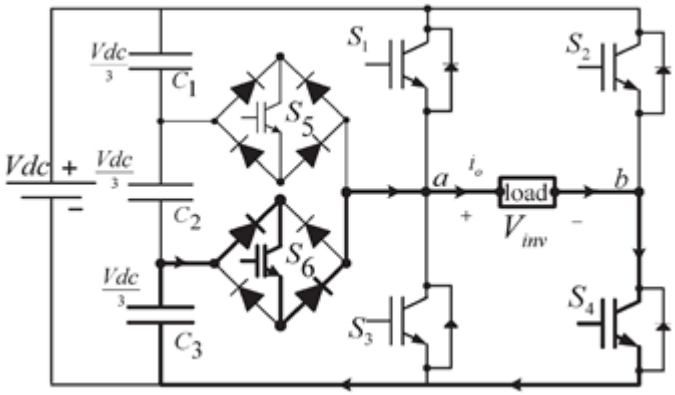
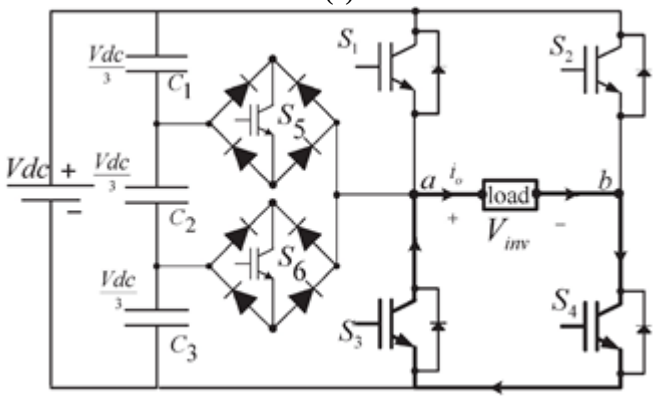


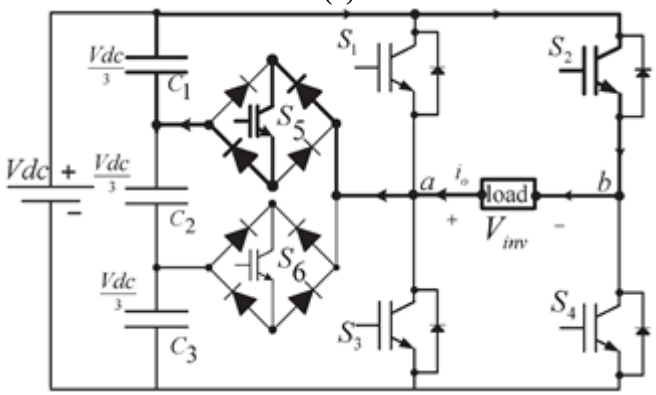
Fig. 2. Switching combination required to generate the output voltage (Vab). (a) Vab = Vdc. (b) Vab = 2Vdc/3.



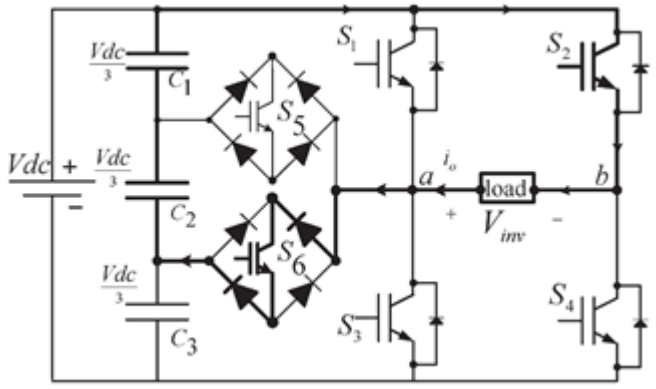
(c)



(d)

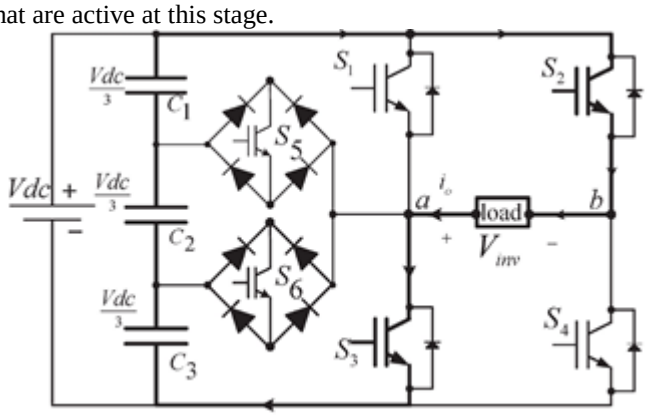


(e)



(f)

other controlled switches are OFF; the voltage applied to the load terminals is −Vdc. Fig. 2(g) shows the current paths that are active at this stage.



(g)

Fig. 2. (Continued.) Switching combination required to generate the output voltage (Vab). (c) Vab = Vdc/3. (d) Vab = 0. (e) Vab = −Vdc/3. (f) Vab = −2Vdc/3. (g) Vab = −Vdc.

TABLE I
OUTPUT VOLTAGE ACCORDING TO THE SWITCHES' ON–OFF CONDITION

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

Table I shows the switching combinations that generated the seven output-voltage levels (0, −Vdc, −2Vdc/3, −Vdc/3, Vdc, 2Vdc/3, Vdc/3).

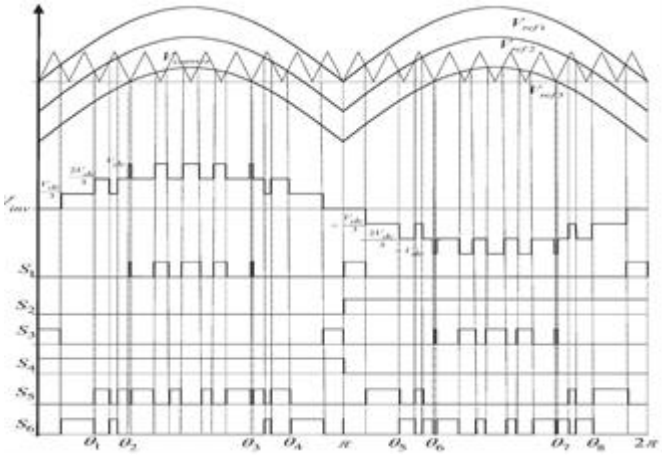


Fig. 3. Switching pattern for the single-phase seven-level inverter

III. PWM MODULATION

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (Vref1, Vref2 and Vref3) were compared with a carrier signal (Vcarrier).

The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If Vref1 had exceeded the peak amplitude of Vcarrier, Vref2 was compared with Vcarrier until it had exceeded the peak amplitude of Vcarrier. Then, onward, Vref3 would take charge and would be compared with Vcarrier until it reached zero. Once Vref3 had reached zero, Vref2 would be compared until it reached zero. Then, onward, Vref1 would be compared with Vcarrier. Fig. 3 shows the resulting switching pattern. Switches S1, S3, S5, and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that was equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 4 shows the per unit output-voltage signal for one cycle. The six modes are described as follows.

$$\begin{aligned}
&\text{Mode 1}: 0 < \omega t < \theta_1 \text{ and } \theta_4 < \omega t < \pi \\
&\text{Mode 2}: \theta_1 < \omega t < \theta_2 \text{ and } \theta_3 < \omega t < \theta_4 \\
&\text{Mode 3}: \theta_2 < \omega t < \theta_3 \\
&\text{Mode 4}: \pi < \omega t < \theta_5 \text{ and } \theta_8 < \omega t < 2\pi \\
&\text{Mode 5}: \theta_5 < \omega t < \theta_6 \text{ and } \theta_7 < \omega t < \theta_8 \\
&\text{Mode 6}: \theta_6 < \omega t < \theta_7 .
\end{aligned} \tag{1}$$

IV. SIMULATION RESULTS

The MATLAB model consists of Cascaded Inverter Bridge, gating pulses, loading arrangement, current measurement and voltage measurement systems and is highlighted in Fig. 5. All required measurements can also be seen in the diagram. It resembles a block diagram structure. R-L load is used in Fig. 5 is replaced by only R load while taking the results with pure resistive load. Each of the subsystem is explained in detail.

The arrangement of IGBT switches along with diodes, DC supply and capacitor arrangement is included in subsystem form and is shown in Fig. 6. It shows six IGBT switches and two diode bridges. IGBTs S1 -S4 are arranged in conventional H-bridge inverter structure while S5 and S6 are arranged along with two diode bridges in cascaded form. This arrangement is same as discussed in section II where operation of inverter was

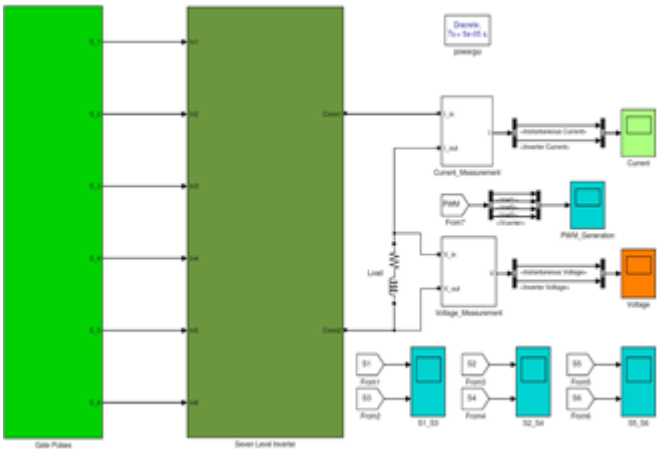


Fig. 5. Seven Level Single Phase Inverter Model in MATLAB Simulink

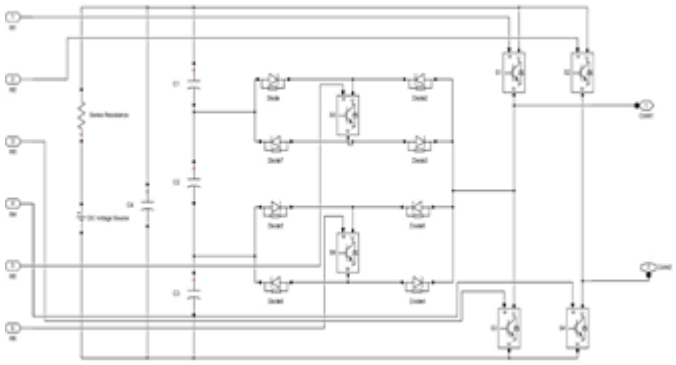


Fig. 6. Seven Level Diode-Clamped Cascaded Inverter

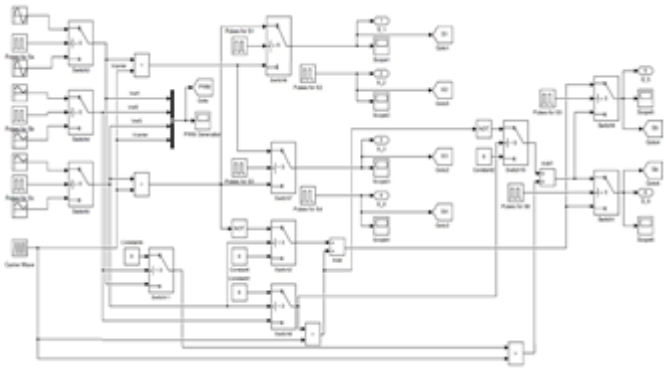


Fig. 7. Seven Level Single Phase Inverter Model in MATLAB Simulink

Discussed. One input capacitor of value 20mF in parallel and three series capacitors of 1mF each are used to generate the required steps for generating the seven level output voltage. DC supply of 220V is given along with a series resistance of 1 ohm to limit the current inrush during capacitor charging. The development of gate pulses to drive these IGBT switches is discussed in Fig. 7

As discussed in section II, a single carrier wave is compared with three reference waves. These three reference waves are generated using three sine wave function blocks in MATLAB Simulink. To obtain positive sine wave even in negative half cycle another three sine wave function blocks are used with 180 deg. phase shift and is passed through a switch timed at end of each half cycle. Thus six sine waves functions are used and only three positive reference waves are generated using switch arrangement. The arrangement of gate pulse development system is shown in Fig. 7. These three reference waves have different biases and are compared to a triangular carrier wave of frequency 2kHz

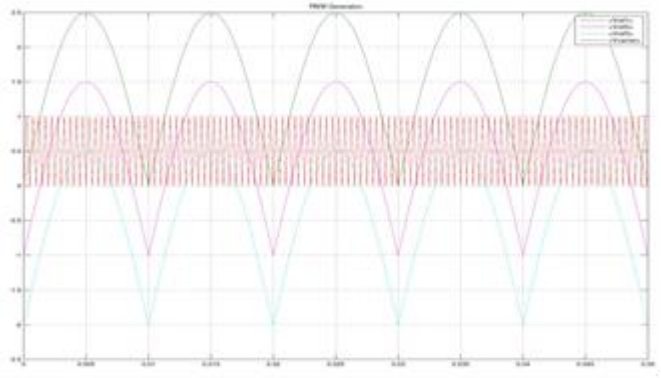


Fig. 8. PWM Generation

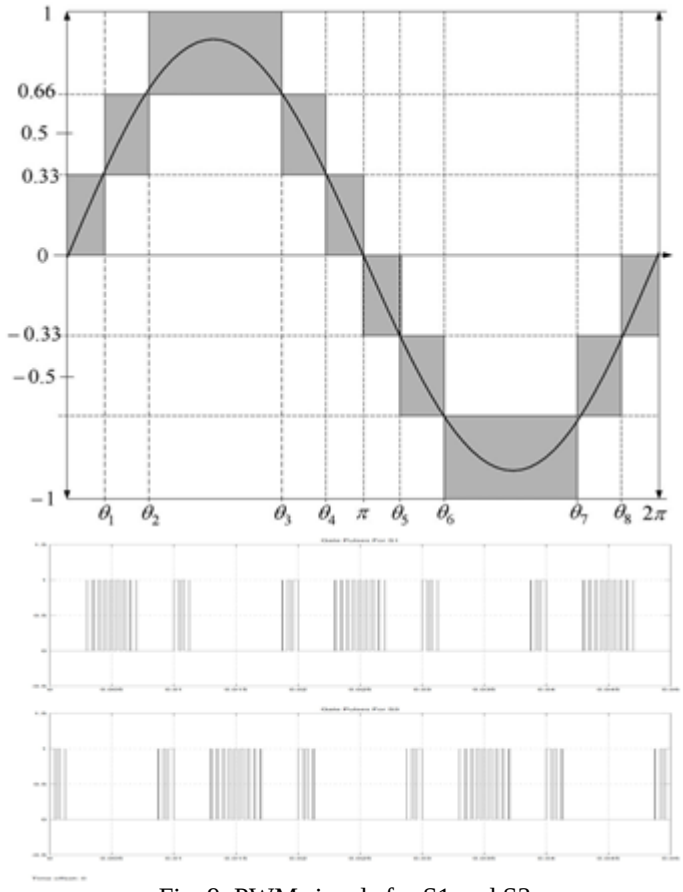


Fig. 9. PWM signals for S1 and S3.

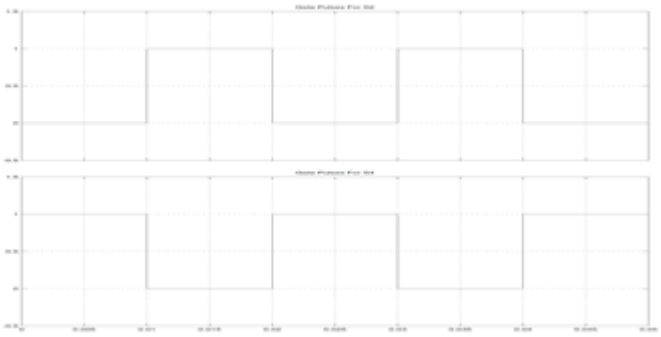


Fig. 10. PWM signals for S2 and S4.

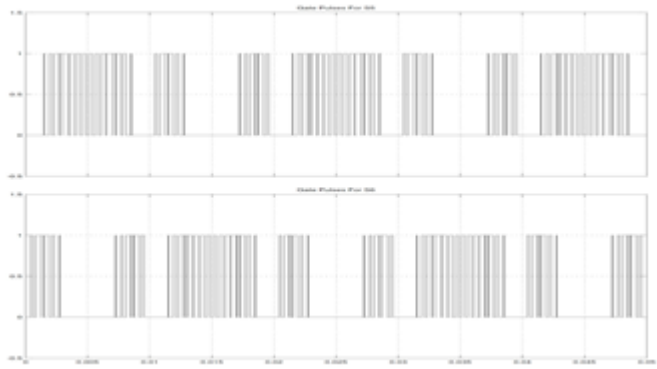


Fig. 11. PWM signals for S5 and S6.

These signals are shown in Fig. 8.

Further the switching pattern is generated for all the six IGBT switches. The gate pattern for IGBT switches S1 and S3 pair, S2 and S4 pair and S5 and S6 pair are shown in Figs. 9, 10 and 11 respectively.

A seven level voltage output waveform is shown in

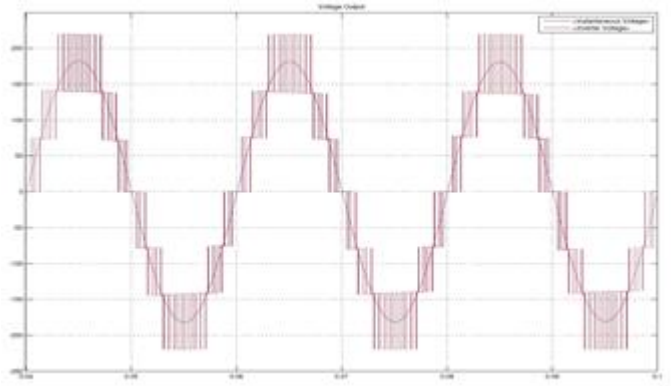


Fig. 12. Output Voltage Waveform

Fig. 12. Seven voltage steps (Vdc, 2Vdc/3, Vdc/3, 0, -Vdc, -2Vdc/3, -Vdc/3) can easily be observed in the figure. It remains same in case of both R and R-L loads. The instantaneous voltage waveform can also be seen in the Fig. 12.

The current waveforms for R load of 100 ohm and R-L load of R = 10 ohm, L = 70mH are shown in Figs. 13 and 14 respectively. Distortions in the current wave form can be observed for R-L load

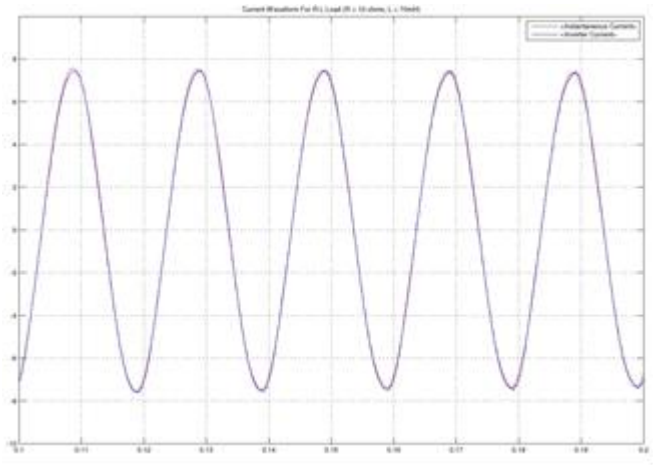


Fig. 14. Current Waveform for RL load.

Fig. 15. THD Analysis of current waveform in case of R Load.

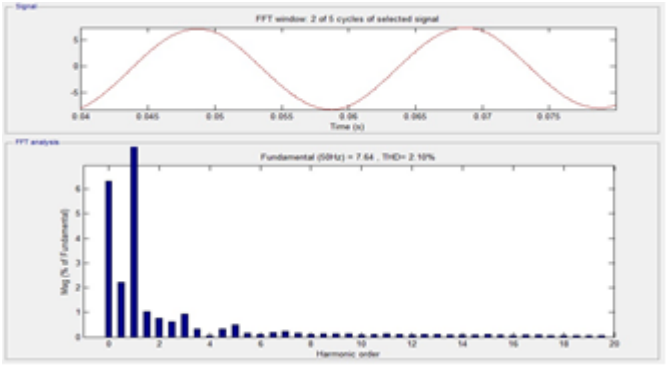


Fig. 16. THD Analysis of current waveform in case of RL Load.

FFT analysis using Nyquist frequency for computation of THD for current wave form in case of R and R-L load is shown in Figs. 15 and 16.

CONCLUSION

A modified H-bridge topology for single phase seven level inverter was discussed in the paper. PWM strategy was used to drive gate pulses of the IGBT switches. Seven output voltage levels were observed in the voltage output waveform. Further, it was seen from Figs. 15 and 16 that THD% for current waveform is below 0.25 in case of R load and below 2.5% during R-L load. Thus it can be concluded that THD is drastically reduced with the proposed seven level inverter system and is suitable for many medium and high voltage applications.

REFERENCES

[1] K. A. Corzine, M. W. Wielebski, F. Z. Peng, and J. Wang, "Control of cascaded multilevel inverters," IEEE Trans. Power Electron., vol. 19, no. 3, pp. 732–738, May 2004.

[2] J. K. Author, J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] E. Villanueva, P. Correa, J. Rodríguez, and M. Pacas, "Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photo-voltaic systems," IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[4] L. M. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[5] J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Unidimensional modulation technique for cascaded multilevel converters," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1058– 1064, Oct. 2002.

[6] S. Vazquez, J. I. Leon, L. G. Franquelo, J. J. Padilla, and J. M. Carrasco, "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source," IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 2513–2521, Jul. 2009.

[7] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimanez, "A new simplified multilevel inverter topology for DC–AC conversion," IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[8] V. G. Agelidis, D. M. Baker, W. B. Lawrance, and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications," in Proc. IEEE ISIE, Guimäes, Portugal, 1997, pp. 589–594.

[9] S. J. Park, F. S. Kang,M.H.Lee, and C. U. Kim, "Anewsingle-phase five level PWM inverter employing a deadbeat control scheme," IEEE Trans. Power Electron., vol. 18, no. 3, pp. 831–843, May 2003.

[10] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid connected PV system employing digital PI controller," IEEE Trans. Ind. Electron., vol. 56, no. 1, pp. 149–158, Jan. 2009.

[11] N. A. Rahim and J. Selvaraj, "Multi-string five-level inverter with novel PWM control scheme for PV application," IEEE Trans. Ind. Electron., vol. 57, no. 6, pp. 2111–2121, Jun. 2010.

[12] N. A. Rahim and K. Chaniago, "Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System," IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.