International Journal of Technical Research and Applications e-ISSN: 2320-8163,
www.ijtra.com Volume 2, Issue 6 (Nov-Dec 2014), PP. 134-138

REALISATION OF STATIC RANDOM ACCESS MEMORY USING QUATERNARY DLATCH

Ch.Chandini, A.Maria Jossy
Dept. of ECE, SRM University, Kattankulathur-603203
chandinichatrathi@gmail.com, jossydeepan@gmail.com

Abstract - Large number of interconnection requirement has become a major limitation to the designs using binary logic. One of the solutions for this is Multiple-Valued Logic (MVL). MVL proves to be advantageous as it reduces dynamic power dissipation, increases computational ability, data density and requires less number of interconnects. In this paper, the implementation of a Static Random Access Memory (SRAM) cell using a quaternary D Latch is proposed. The D Latch is built using NMAX, NMIN and quaternary inverter circuit. Using this SRAM cell a 4X4 SRAM array is constructed and is compared with 4X4 array of Quaternary Static CMOS memory cell. The spice coding is done using 0.18µm CMOS technology and verification of the design is done through HSPICE and COSMOSSCOPE Synopsis Tools. Power and delay of the circuit is analyzed.

Index Terms – Multiple Valued Logic(MVL), NMAX/NMIN Quaternary. Inverter Circuit

I. INTRODUCTION

In modern SOC design, the interconnection is becoming a major problem because of the bus width. This problem can be solved by using Multiple-valued logic interconnection [1]. For example a conventional 16 – bit bus (0 and 1) represents 65536 combinations. If we code the output with Quaternary logic (0, 1, 2 and 3), the width of the bus is reduced from 16 to 8. As a result, we can reduce power and area requirement for the interconnection.

Moore's law states that number of devices per unit area increases exponentially. But the IC industry must solve many problems to maintain this exponential growth. The problem entails interconnection (both on chip and between chips), packaging and cooling. Routing of interconnections on chips is well known as a major problem, and silicon area used for interconnections may be greater than that used for active logic elements.

The use of circuits with more than two levels has been offered as a solution to these interconnection problems [2].To realize m-valued ICs, a serious and fair comparison between 2- valued and m-valued ICs is required according to VLSI criteria. For IC manufacturers the first criterion is money: Silicon (chip area) is money; time (design time) is money. Thus performance of integrated circuits is a tradeoff between several criteria; speed, power dissipation, chip area, yield, CAD programs for IC design and so forth.

II. MULTIPLE VALUED LOGIC MEMORIES

Memory application is an area where the multi-valued approach has been successfully used to design commercial integrated circuits. Read-only memory designs by Intel, Motorola, and General instrument, and random access memory (RAM) design by Hitachi have been presented. With memories the basic objective is to reduce chip area, while retaining acceptable timing characteristics. [3].

A technique has been presented by David A Rich [4] to encode two bits of information in a single cell location of read-only memory by varying the threshold voltage of the memory cells with multiple ion implants. Voltage-mode CMOS multiple valued logic circuits have been realized in a standard 2 micron p-well poly-silicon gate CMOS technology in [5] by K.W. Current, A novel methodology designing for Multi-valued logic voltage mode storage circuits was introduced in [6] by I. Thoidis. Using the proposed inverter based unit, uni-signal controlled pass gates and true single phase clocked logic based output units, efficient r- bit dynamic and pseudo-static latches can be designed. The conventional flip-flop core was generalized to multi stability in full static CMOS without compromising the standard binary CMOS features such as ratio less device sizing, negligible static power consumption and wide noise margins by Ugur Cilingiroglu [7].

A lack of CMOS-compatible multiple-valued static storage technique has been recently confirmed in a review, which excludes static RAM from the list of proven multiple-valued memory techniques but includes such non static techniques as EEPROM, ferroelectric, and dynamic RAM [8]. A very similar application pattern exists in the specific area of synaptic memory design for adaptive neural networks. The need for analog storage has been fulfilled with multiple-valued storage in EEPROM structures [9]–[13] or in refreshed capacitors [14]–[17].

III. QUATERNARY D LATCH

The D Latch circuit is built using MIN gate (OR gate in binary), NMAX gate (AND gate in binary) and quaternary inverters as shown in figure 1. When en is equal to logic 3, the latch is open and the output follows the input. When en is equal to logic 0, the latch is closed and the output is held constant. The output of the MIN gate circuit is the input to the NMAX gate. The outputs of NMAX circuit are d and q which have quaternary logic levels.

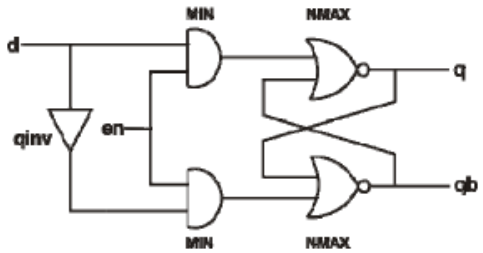


Figure 1: Quaternary D Latch

IV.QUATERNARY INVERTER

A quaternary inverter circuit (figure 2) that accomplishes the logic described in the truth table in Table 1. The inverter consists of three PMOS and three

NMOS transistors. In the case of three different *V*DD, one can connect transistor sources in 0, 1, 2, or 3 V, and the real threshold values depend on this connection.

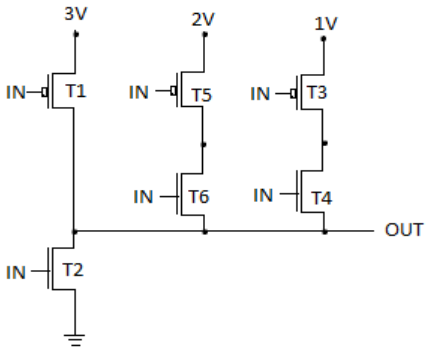


Figure 2: Quaternary Inverter

If the input value is 0V, transistor T1 is turned on, driving the output to 3V, whereas T2, T4, and T6 are turned off, cutting the remaining path. When the input is set to 1 V, T1 is turned off, whereas T6 is turned on, driving the output to 2 V. When the input is set to be 2 V, T5 is turned off, whereas T4 is turned on, hence driving the output to 1 V. T2 sinks the output to zero only when the input goes to 3 V, turning off T3.

Table 1: Quaternary inverter Truth Table

INPUT	OUTPUT
0	3
1	2
2	1
3	0

The threshold voltage of each transistor in the quaternary inverter is given in the Table 2.

Table 2: Transistor Threshold Voltages

	T1	T2	T3	T4	T5	T6
Vt	-2.2	2.2	1.8	0.2	-0.2	-1.8
Type	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS

A. MIN CIRCUIT

In quaternary logic, the AND/NAND logic gates are replaced by MIN/NMIN gates. The MIN operation sets the output of the MIN circuit to be the lowest value of several inputs. The implementation of a MIN circuit with two quaternary inputs is shown in Figure 3. The circuit is based on the inverter circuit in Figure 2 and a common binary NAND circuit.

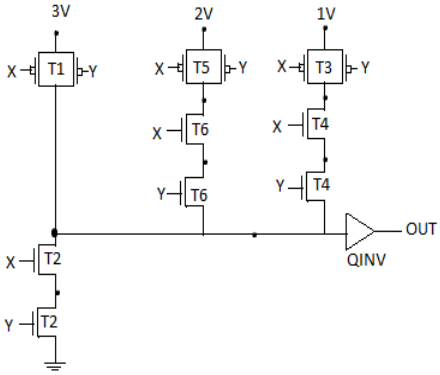


Figure 3: MIN circuit

An input set to zero will produce the output of 0 V regardless of the other input voltage level. The NMOS transistors disposed in series make the paths to 1 V, 2 V, and ground to be opened only when both inputs are equal to or higher than the *Vt* of both transistors. PMOS transistors are responsible to close the path when both inputs are higher than their *Vt* values. Table 3 shows the truth table of the MIN gate.

Table 3: MIN circuit truth table

Y \ X	0	1	2	3
0	0	0	0	0
1	0	1	1	1
2	0	1	2	2
3	0	1	2	3

B. NMAX CIRCUIT

Logic gates OR and NOR also have no meaning in quaternary logic, and these gates are replaced by MAX and NMAX gates, respectively. The MAX gate is a circuit of multiple inputs and sets the output in the higher value of all entries. Figure 4 shows an NMAX circuit with two quaternary inputs, designed for voltage-mode quaternary CMOS logic.

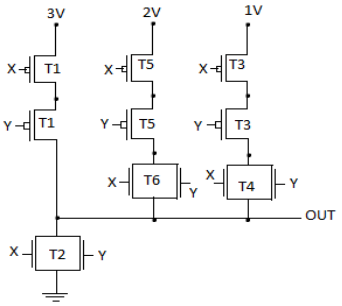


Figure 4: NMAX circuit

The highest value of all the inputs sets the output. When both inputs are in 0 V, both T1 transistors are turned on, driving the output to 3 V. One of the inputs set on a higher value is enough to close the path from the output to the 3V power supply and to open all other paths. Any input in 1 V opens one of the T6 transistors and turns off one of the T1 transistors, placing the output at 2 V. In the same way, any 2V inputs will turn on any T4 transistor while at the same time turning T1 and T5 off. Any 3V input turns on a T2 transistor and turns off the T1, T5, and T3 transistors. The truth table of NMAX gate is shown in Table 4.

Table 4: NMAX circuit truth table

Y \ X	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

V. QUATERNARY SRAM CELL

Memories are said to be static if no periodic clock signals are required to retain stored data indefinitely. The basic requirements of the SRAM cell can be summarized in two points, data should not get modified during read operation and data has to be modified during write operation.

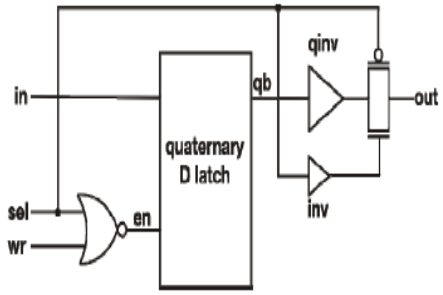


Figure 5: Quaternary SRAM cell

To build up the Quaternary SRAM cell as shown in figure 5 a quaternary D latch and a tri state buffer (figure 6) are used.

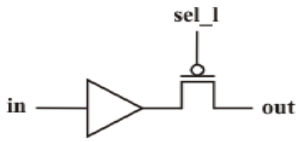


Figure 6: TriState Buffer

The tristate buffer is implemented by connecting a quaternary inverter in series with a pass transistor as shown in figure 6. The pass transistor used is essentially a PMOS transistor. The gate of the PMOS transistor is connected to sel_l input. Working is as given in Table 5.

Table 5: Tristate Buffer Truth Table

Sel_1	PMOS state	OUT
0	On	In_bar
1	Off	Z

'Sel' is the select input and 'wr' is the write enable input of the SRAM cell. When sel=1, the SRAM cell is disabled and when sel=0 the SRAM cell is enabled**.**

Write Operation: During write operation, wr=0. The output of the NOR gate is logic high. Therefore the latch is enabled. Thus the input is written into the SRAM cell.

Read Operation: During read operation, wr=1. The sel signal of NOR gate is 0. Therefore the latch is disabled. Thus the output is read from the SRAM cell. The table 6 summarizes the working of the SRAM cell.

Table 6: Working of Quaternary SRAM cell

sel	wr	SRAM operation
0	0	write
0	1	read
1	0	disabled
1	1	disabled

VI. 4X4 QUATERNARY SRAM MEMORY ARRAY

A 4X4 quaternary SRAM array consists of 16 quaternary SRAM cells, a 1X4 decoder and an output driver as shown in the figure 7.

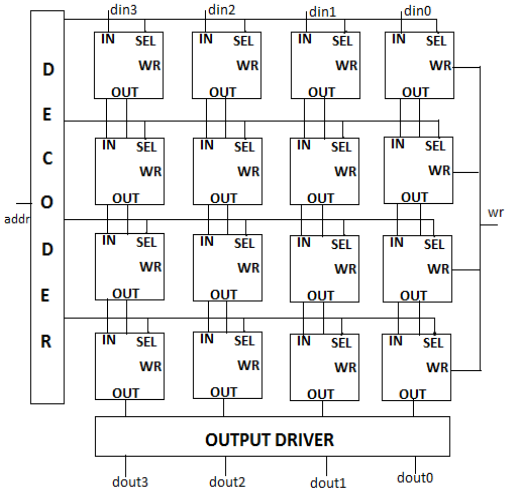


Figure 7: 4X4 SRAM Array

VII. 1X4 DECODER

The address decoder is constructed using down literal circuits (DLC) [18], binary xor gates and binary inverters as shown in the figure 8. The truth table for the decoder is as shown in table 7.

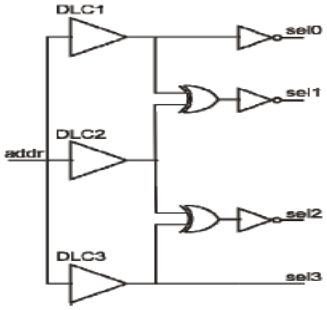


Figure 8: 1X4 Decoder

Table 7: 1X4 Decoder Truth Table

addr	Sel0	Sel1	Sel2	Sel3
0	0	1	1	1
1	1	0	1	1
2	1	1	0	1
3	1	1	1	0

Down literal circuits are realized from basic inverter by changing the threshold voltages of PMOS and NMOS transistors used in the basic inverter. This can be done during the fabrication of the inverter circuit. In the present discussion we will be using 3 different DLC circuits. They are:

- DLC1: vtp= -2.2V and vtn=0.2V.
- DLC2: vtp= -1.2V and vtn=1.2V.

- DLC3: vtp= 0.2V and vtn=2.2V.

VIII. OUTPUT DRIVERS

Output drivers are essentially quaternary inverters in the following 4x4 memory array; there are 4 drivers, one for each output line.

Based on the input address, a particular row of SRAM cells are enabled. din3, din2, din1, din0 constitute the input data write bus. dout3, dout2, dout1, dout0 constitute the output read bus. Based on the address on the address line a particular row of SRAM cells are enabled and wr is the write signal.

IX. RESULTS AND DISCUSSIONS

The above stated SRAM cell and 4x4 arrays was coded and tested using the tools: Synopsys HSPICE Z-2007.03**,** Synopsys Cosmos Scope Z-2007.03-SP1**.** The simulation results of quaternary SRAM cell and SRAM array are shown in figure 9 and 10 respectively.

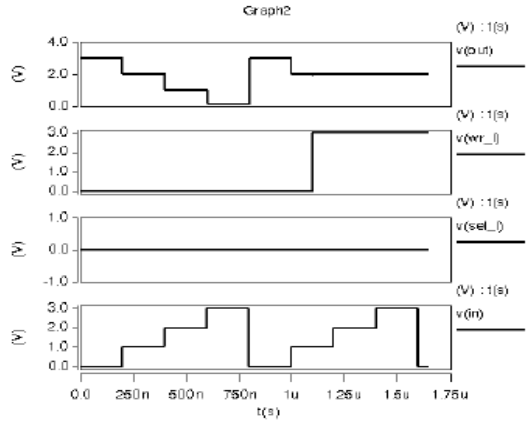


Figure 9: Simulation of SRAM cell

For comparison purpose we have chosen Multiple-valued Static CMOS memory cell [7] and constructed 4X4 array. Simulation is carried out at 180nm technology. Table 8 shows the analysis for single Multiple valued Static CMOS memory cell at 180nm. Average power dissipation is maximum of 226nW when 3V is stored. Delay between write signal and the Vout is in terms of pico secs.

Table8: Quaternary Single Static CMOS Memory cell

Input Voltage (volts)	Average Power (watts) nw	Delay (wrt vs vout) ps
0	0.28	366.96
1	57	160.92
2	148	338.94
3	226	36.65

Table 9 shows the response of output for the write signal in a 4x4 Static CMOS memory Cell array at 180nm. Table 10 shows the average power dissipation including all 4 logic levels and for the whole array. It is 58.91 μW at 180 nm.

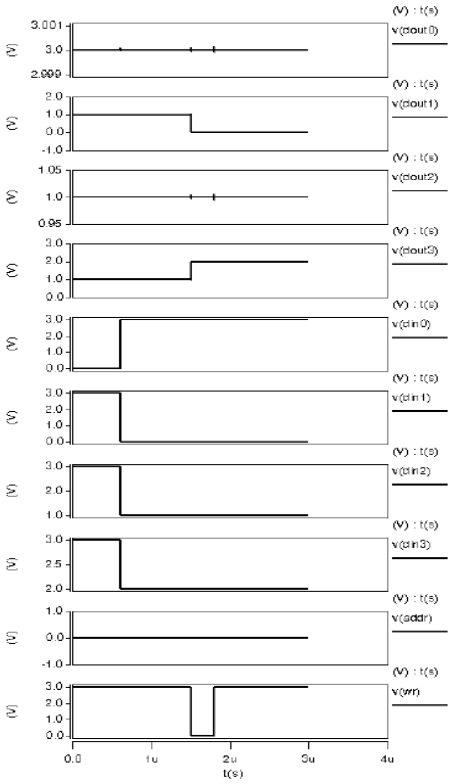
Table 9:4X4 array of quaternary Static CMOS memory cell

Input Voltage (volts)	Average Power (watts) nw	Delay (wrt vs vout) ps
0	2.807	5.531
0.4	0.55	15.427
0.8	3.671	7.105
1.2	11.26	6.161

Table 10: Dynamic Power Dissipation for the whole array

Input Voltage (volts)	Delay (wrt vs vout) ps
0	376.52
0.4	195.78
0.8	815.23
1.2	540.78

Figure 10: Simulation results Quaternary SRAM 4X4 array



Proposed 4x4 quaternary SRAM array shown in table 11 is based on quaternary D latch and is simulated using 180nm TSMC technology files.

Table 11: Proposed 4X4 Quaternary SRAM Array

Power	In uw
Average	9.153

Average power dissipation for the whole array including all four logic levels is given in table 12. It shows 65.28% of improvement in average power dissipation when compared to 4x4 array of Quaternary Static CMOS memory Cell at 180nm.

Table 12: Dynamic power dissipation of Proposed 4X4 Array

Power	In uw
Average	20.45

Binary 4X4 memory array with 0 and 1.2 V as two logic levels is constructed and power analysis is given in table 13.

Table 13: Dynamic power dissipation of binary 4X4 Array

Power	In uw
Average	84.39

Proposed work shows 75% improvement over binary 4X4 array. And also proposed work shows less delay.

X. CONCLUSION

In this paper, 4X4 quaternary SRAM memory array is designed and simulated using a single 1 X 4 decoder, driver and 16 SRAM cells. 4X4 array of quaternary static CMOS memory cell is also constructed and analyzed for average power dissipation and propagation delay using 180nm technology. Quaternary D latch based SRAM array shows 65.28% of improvement in average power dissipation and reduced propagation delay when compared to 4x4 array of Quaternary Static CMOS memory Cell and 75% improvement over binary 4X4 array at 180nm. Proposed new design is appropriate to be applied for the construction of large low power high performance memory circuit design in quaternary logic.

REFERENCES

[1] K. C. Smith, "The prospects for multi-valued logic: A technology and applications view," IEEE Trans. Computers, vol. C-30, no. 9, pp. 619–634, Sep. 1981.

[2] Michitak, "Toward the age of beyond binary electronic systems", Proceedings of 20th international symposium on multiple-valued logic, pp. 162-166, May 23-25, 1990.

[3] Daniel Etiemble etal.Comparison of Binary and Multivalued ICs according to VLSI criteria, Portal Vol 21 Pages: 28 – 42 April1988.

[4] David A Rich et. al., "A four-State ROM Using Multilevel process Technology", IEEE Journal of solid Stata circuits, Vol.Sc-19, No 2, April 1984.

[5] K.W. Current, Memory circuits for Multiple Valued Logic voltage Signals 52 -57 25th IEEE International Symposium on Multiple-Valued Logic 1995.

[6] I. Thoidis et.al Design methodology of Multiple-valued logic Voltage mode storage circuts in Proc. IEEE Int. Symp. Circuits and Systems, vol. 2, 1998, pp. 125–128.

[7] Ugur Cilingiroglu and Yaman ozelci Multiple Valued static CMOS Memory IEEE Transactions on circuits and systems, Analog and digital signal processing. Vol. 48, No 3 march 2001.

[8] Ki-Whan Song et.al Complementary self-Biased Scheme for the robust design of CMOS/SET Hybrid multi-valued logic. Proceedings of the 33rd IEEE International Symposium on multi-valued logic.(ISMVL 2003).

[9] A. Kramer, V. Hu, C. K. Sin, B. Gupta, R. Chu, and P. K. Ko, "EEPROM device as a reconfigurable analog element for neural networks," in Tech. Dig. IEEE IEDM, 1989, pp. 259–262.

[10] D. A. Durfee and F. S. Shoucair, "Comparison of floating gate neural network cells in standard VLSI CMOS technology," IEEE Trans. Neural Networks, vol. 3, pp. 347–353, 1992.

[11] A. J. Montalvo, R. S. Gyurcsik, and J. J. Paulos, "Toward a general-pur- pose analog VLSI neural network with on-chip learning," IEEE Trans.Neural Networks, vol. 8, pp. 413–423, 1997.

[12] D. Fujita, Y. Amemiya, and A. Iwata, "Characteristics of floating gate device as analog memory for neural networks," Electron. Lett., vol. 27, pp. 924–926, 1991.

[13] T. Shibata, H. Kosaka, H. Ishii, and T. Ohmi, "A neuron-MOS neural network using self-learning-compatible synapse circuits," IEEE J. Solid-State Circuits, vol. 30, pp. 913–922, 1995.

[14] D. B. Schwartz, R. E. Howard, and W. E. Hubbard, "A programmable analog neural network chip," IEEE J. Solid-State Circuits, vol. 24, pp.313–319, 1989.

[15] B. Hochet, "Multivalued MOS memory for variable-synapse neural net- works," Electron. Lett., vol. 25, pp. 669–670, 1989.

[16] R. Castello, D. D. Caviglia, M. Franciotta, and F. Montecchi, "Self refreshing analog memory cell for variable synaptic weights," Electron. Lett., vol. 27, pp. 1871–1872, 1991.

[17] E. Sackinger, E. Boser, J. Bromley, Y. Lecun, and L. D. Jackel, "Application of the ANNA neural network chip to high-speed character recognition," IEEE Trans. Neural Networks, vol. 3, pp. 498–505, 1992.

[18] Vasundara Patel K S, K S Gurumurthy, "Design of 4 valued logic flip-flop based on down literal circuit", International Conference on Convergence of Science and Engineering in Education and Research – A Global Perspective in the New Millennium. ICSE 2010, 21 - 23, April 2010.