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PERFORMANCE EVALUATION OF THE SECOND GENERATION CURRENT CONTROLLED CONVEYOR (CCCII) AND ANALYSIS OF SIMPLE VOLTAGE AND CURRENT AMPLIFIER BASED ON IT

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Abstract- This paper describes the architecture of second generation current conveyor (CCCII)and designing an amplifier using second generation current conveyor. The designed amplifier through CCCII+ can be used in various analog computation circuits and is superior in performance than the classical opamp. It provides better gain with higher accuracy. The presented approach over here is to design current amplifiers and voltage amplifiers using current controlled current conveyor (CCCII). The second generation CCCII has the advantage of electronic adjustability over the CCII i.e. in CCCII, the X-terminal intrinsic resistance can be adjusted througha bias current is possible. The CCCII has been designed to work both as current amplifier and voltage amplifier. Various simulations have been carried out to obtain the desired results.

Key words: Amplifier, Current controlled conveyor, DOCCCII, Tunable current amplifier, Tunable voltage amplifier.

I. INTRODUCTION

In the field of signal processing Current conveyors are most promising device and have the features like high bandwidth, greater linearity, larger dynamic range, low power consumption, simple circuitry and occupy less chip area. The second generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII i.e. in CCCII; adjustment of the X-terminal intrinsic resistance via a bias current is possible. The CCCII has been designed to work both as current amplifier and voltage amplifier. Various simulations have been carried out to obtain the desired results. The *outcomes show good results and an amplified waveform has been obtained in both the cases.*

II. THE SECOND GENERATION CURRENT CONVEYOR (CCII)

The second-generation current-conveyor was developed by Sedra in 1970. A current conveyor is a building block similar to an operational amplifier and capacitors and diodes, can implement several useful analog sub-systems such as amplifiers, integrators, and rectifiers. which, when used in conjunction with other components such as resistors, The second generation current conveyor is a three terminal device. Its symbol is shown in figure 1.

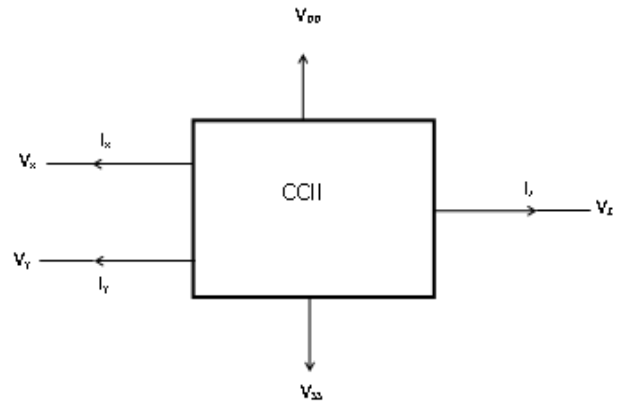

Fig.1 Current ConveyorSymbol and Characteristic

The current conveyor's response is given by equat ion

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm\beta & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad \text{……(1)}$$

Impedance is finite and must be taken into consideration in the circuit design. When a voltage is applied at node Y, that voltage is replicated at node X. This is similar to the virtual short on an op-amp. Also when a current is injected into node X, that same current gets copied into node Z. The notation CCII+ denotes a positive Z output current conveyor (= + 1) whereas CCII- denotes a negative Z output current conveyor (= - 1). Thus the terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive polarity (in CCII+) or negative polarity (in CCII-). One model used to analyze a CCII+ is shown in figure 2. The op-amp in unity-gain feedback configuration ensures that V_x is equal to V_y, and the current mirrors ensure that I_z is equal to I_x. Here the op-amp's output stage has infinite output impedance.

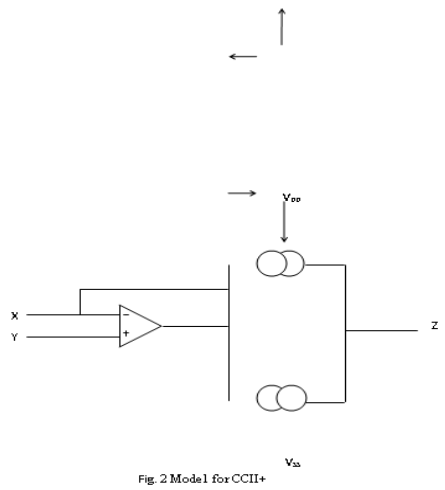

Fig. 2 Model for CCII+

III. AMPLIFIER & Its ANALYSIS

A. Tunable Voltage Amplifier

An electronic circuit whose function is to accept an input voltage and produce a magnified accurate replica of this voltage as an output voltage. The voltage gain of the amplifier is the amplitude ratio of the output voltage to the input voltage.

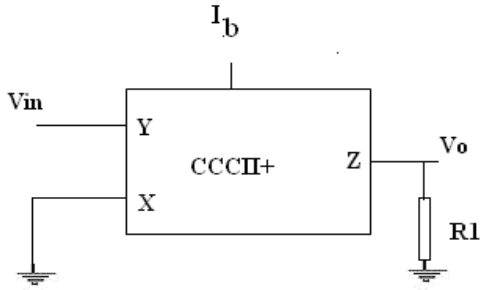

Fig.3 Circuit of Tunable Voltage Amplifier

The analysis of the amplifier circuit [9] shown in Figure 3 is as follows;

We know for CCCII+

$V_Y = V_X + I_X R_X$ .....(2)

Since $V_X = 0$, $V_Y = V_{IN}$ ……..……....(3)

$V_0 = I_Z R_1 = I_X R_1$……..…….(4)
$V_0 = V_{IN}(R_1/R_X)$……..……....(5)

Where R_X depends on bias current I_b.

For realization, of the above voltage amplifier, CMOS design of CCCII+ is adopted, and the voltage amplifier of figure 3 is simulated on HSPICE .The input voltage is applied at node Y of the CCCII+ of the magnitude of 4mV peak to peak. The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10μA.The simulation results of the voltage amplifier are presented in Figure 4. The output obtained after the simulation is of value 38.4mV (peak to peak). The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10μA and theoretically 10 is selected as the gain of the voltage amplifier.

The simulation results of the voltage amplifier are presented in Figure 4. The output obtained after the simulation is of value 38.4mV (peak to peak) that means the practical value of gain is 9.6.

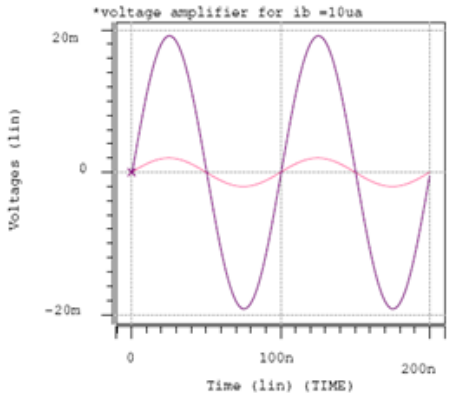

Fig. 4 Graph for Transient Response of Amplifier for f=10MHz

Figure 5 shows the frequency response of the above mentioned amplifier. AC analysis is performed to know about the bandwidth which is an important parameter and can be determined as the frequency at which the power of the load is at least 50%.This condition in absolute units corresponds to 70.7% and 3 dB in decibels units.

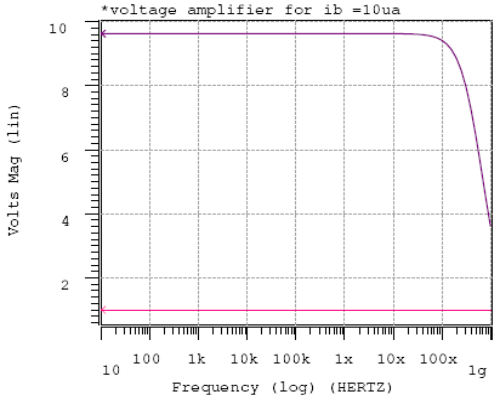

Fig.5 Frequency Response of Amplifier

B. Tunable current amplifier

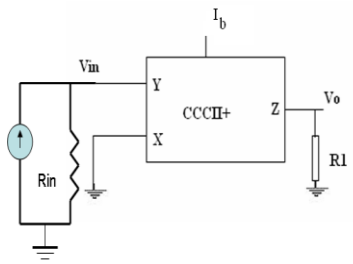

Fig.6 Circuit of Tunable Current Amplifier

The analysis of the current amplifier circuit shown in fig 6 is as follows

We know for CCCII+

$V_Y = V_X + I_X R_X$……..(6)

Since $V_X=0$,

$V_Y = I_X R_X = I_{IN} R_{IN}$……..…(7)

$I_X = I_{IN} R_{IN}/R_X = I_Z$……...(8)

Current Gain $A=I_Z/I_{IN}= R_{IN}/R_X$…….....(9)

For realization, of the above current amplifier, CMOS design of CCCII+ is adopted, and the current amplifier of fig 6 is simulated on HSPICE .The input current is applied at node Y of the CCCII+ of the magnitude of 2µA peak to peak. The output is seen on Z+ node of the conveyor. The bias current I_b is taken as 10µA. The simulation results of the current amplifier are presented in Fig 7. The output obtained after the simulation is of value 18.8 µA (peak to peak).

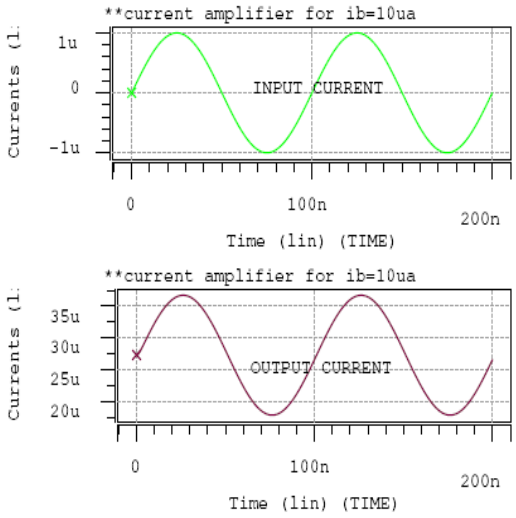

Fig. 7 Transient analysis for current amplifier

Figure 8 given below shows the frequency response of the above mentioned amplifier. AC analysis is performed to know about the bandwidth which is an important parameter and can be determined as the frequency at which the power of the load is at least 50%.This condition in absolute units corresponds to 70.7% and 3 dB in decibels units.

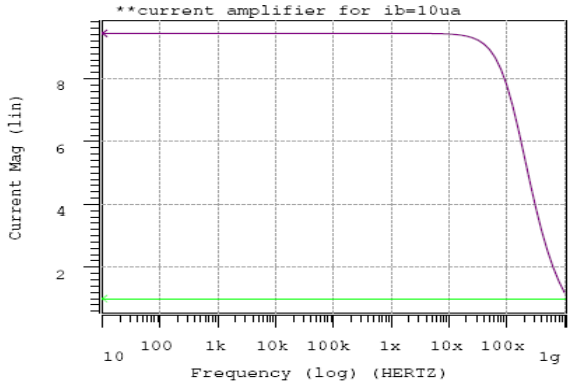

Fig 8 Frequency response for Current Amplifier

IV. SIMULATION & IMPLEMENTATION RESULTS

Some Simulation results shown above in Figures 4, 5, 7 & 8 respectively.

Table 1 shows values of the voltage gain with bias current in µA The graph shown below in figure 9 is plotted across the voltage gain to the device bias current in µA . As can been seen from the graph that the voltage gain increases with the increase in device bias current I_b. As bias current varies from 0 µA to

100 µA, voltage gain increases from 1.1 to 1.8.

Table 1-Voltage gain Vs Bias Current

S.No.	Bias Current(I_b) in	Voltage Gain
1	5	1.1
2	10	1.22
3	20	1.35
4	30	1.46
5	50	1.58
6	70	1.69
7	90	1.77
8	100	1.8

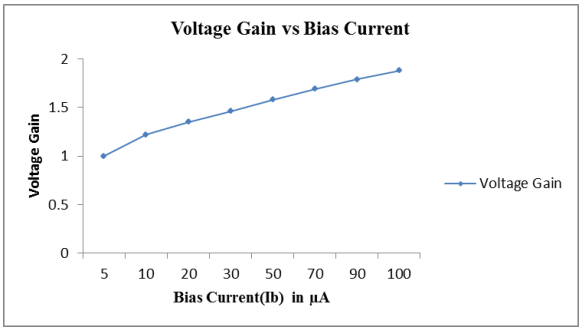

Fig. 9. Graph between Voltage Gain & Bias Current, R_1=1K constant

V. CONCLUSION

Current-mode circuits are undoubtedly the most widely accepted operational devices in continuous time and current mode signal processing. In addition a number of novel circuit functions such as amplifier, integrator, summer, differentiator, etc. and topologies like filters and oscillator have been explored on a front of current mode analogue circuits, opening up wider area of interest.

The circuit of CCCII+ is verified through HSPICE simulation results. The circuit of CCCII+ and the designed amplifier is verified through HSPICE simulation results.

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