International Journal of Technical Research and Applications e-ISSN: 2320-8163,
www.ijtra.com Volume 4, Issue 3 (May-June, 2016), PP. 210-214

DESIGN OF LOW POWER TEST PATTERN GENERATOR FOR BUILT IN SELF-TEST (BIST) CIRCUITS

Arun Kumar
M.Tech, Sharda University
Greater Noida, U.P
arun31singh@gmail.com

Abstract— **Low Power consumption has become growing larger for communication systems and battery operated devices. These are laptop computers, multimedia products, and cell phones. For this battery operated devices, the energy consumption is a critical issue for design since it affect the batteries life. Thereby, the reduction of the energy consumption is become one of the most growing topics in the electronics industry and it is the most challenging areas of research. In the present time, modern design and technologies external testing become more difficult. Therefor built-in self-test has to rise as a sign of future excellence solution to the testing problem. BIST is a design for testability methodology to find out faulty elements in a system by incorporate test logic on-chip. A modern low power test pattern generator is using a linear feedback shift register (LFSR), called LP-TPG, is presented to reduce the average and peak power of a digital circuit during test. The test patterns generated by LP-TPG are more than conventional LFSR. The objective of having intermediate patterns is to reduce the internal activities of primary inputs which decrease the switching activities in the circuit under test (CUT), and power consume. The irregular nature of the test patterns is holding on perfect. The area over the additional components to the LFSR is significant compared to the large circuit sizes. The experimental results are shown verify up to 63% and 20% reduction in average and peak power, respectively.**

Index terms- **Logic Built in Self-Test, L F S R, Low power Test Pattern Generation.**

I. INTRODUCTION

Power Dissipation is a challenging problem in modern System-on-Chips Design and Testing. In VLSI circuits, built in self- test (BIST) are used for testing. The function of the BIST is to reduce power dissipation without affecting to the fault coverage .The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices, daily life equipment's, and communication system are increasing rapidly.

Built-in self-test is a design technique where parts of a circuit are used to test the circuit itself. Built in self-test is the capability of the circuit to test itself. BIST represents converge of concept of built in test and self -test and hence come to be synonymous with these terms.

The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing.

Four reasons are responsible for power increase during test.

- High switching activity due to test patterns
- Parallel activation of internal cores during test
- Power consumed by extra DFT circuitry
- Low correlation among test vectors

Main purpose of testing is to detect malfunctions in the hardware of product and to locate their reason so that they may be eliminated. In others words the aim of testability is to do the parts testable not only on test fixtures particular from the system but also within the system when the parts are connected. Design for test, DFT must be a central element of any design process these days. With circuit promiscuity protrude and component size decreasing, the testability of electronic circuits is more deciding as testing is becoming ever more demanding. The only way that tolerable testing can be obtain by employing design for test.

DFT is a technique, which facilitates a design to become testable after production. Its the extra reasonable which we put in the simple design, during the design process, which helps its post-production testing before production testing is must because, the process of production is not 100% error free. There are fault in silicon which contribute to the fault in the device.

II. LITERATURE SURVEY

Many low power testing techniques have been proposed:-

- The External Testing techniques include the methodologies based on Automatic Test Pattern Generator (ATPG), Vector Reordering. ATPG algorithms can broadly be classified into random and deterministic algorithms.[1]

    1. Random ATPG algorithms involve generation of random vectors and *test efficiency* (test quality quantified by fault coverage) is determined by fault simulation.
    2. Deterministic ATPG algorithms generate tests by processing a structural net list at the

logic level of abstraction using a specified fault list from a fault universe.

- Y. Bonhomme P. Girard is developed a new low power scan-based BIST technique which can reduce the switching activity during test operation. The proposed low power /energy technique is based on a gated clock and the clock tree. The idea is to reduce the clock frequency on the cells during shift operations without increasing the test time [6].
- Architecture whereas the BIST include techniques based on LFSR, Test Scheduling, Circuit Partitioning and Reseeding.
- **Circuit partitioning:** Low-power BIST strategy based on circuit partitioning was proposed by Girard [11]. This strategy partitions the original circuit into two structural sub circuits so that two different BIST sessions can randomly test each other circuit.
- **LFSR reseeding** is an attractive approach for compressing test data. The proposed deterministic BIST scheme provides a way to reduce test power for LFSR reseeding. By *Scan slices overlapping* haved with LFSR reseeding, it can reduce transitions during test (up to 90%) and specified bits in test cubes [8].

- **LOW-POWER TEST PATTERN GENERATORS:**

  - Zhang, Roy, and Bhawmik proposed modifying the LFSR by adding weight sets to modulate the pseudorandom vector's signal probabilities and thus decreased energy consumption and increased fault coverage [15].
  - A low-power test pattern generator was presented by Corno [14] which base the test pattern generation on cellular automata and designs it to effectively reduce test power in combinational circuits until attaining high fault coverage. Testing time and area covered remain intact.

III. METHODOLOGY FOR ARCHITECTURE FOR BIST

Built-In Self -Test (BIST) is the most convenient approach for low power testing as it provides a larger range for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG). The LFSR generates all possible test vectors with the appropriate use of tap sequence. Even the pseudorandom behaviour of the LFSR reduces the correlation among test vectors which means that it can achieve high fault coverage in a relatively short run of test vectors.

A. BIST Implementations

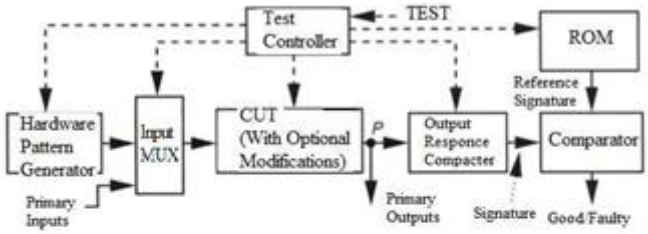


Fig3.1(a): BIST .

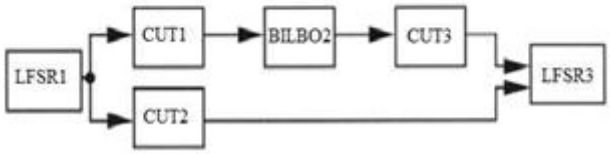


Fig3.1(b): Complex BIST implementation

A BILBO is a bank of D flip-flops in the CUT that has test hardware added to make it behave in one of four modes:

• As ordinary D flip-flops.

• As a linear feedback shift register (LFSR) hardware pattern generator.

• As an LFSR configured to compact a circuit response.

• As a scan chain.

B. BIST Pattern Generation

The following hardware pattern generation approaches have been used [1].

1. **ROM**.- One method is to store a good test-pattern set (from an ATPG program) in a ROM on the chip.

2. **LFSR**.- Another method is to use a linear feedback shift register (LFSR) to generate pseudo-random tests.

3. **Binary Counters-**. A binary counter can generate an entire test sequence, but this can use very much test time if the number of inputs is very large.

4. **Modified Counters**. Modified counters have also been successful as test-pattern generators, but they also go for long test sequences.

5. **LFSR and ROM**. For primary test mode, the most effective approaches is to use an LFSR to generate test-patterns with an ATPG program. These additional test-patterns can either be stored in a ROM on the chip for a second test, they can be applied in a scan chain in order to logic the stuck-fault coverage to 100%.

6. **Cellular Automaton**. In this approach, each pattern generator cell has a logic gates, a flip-flop to connections only to neighbouring gates. The cell is respond to produce the cellular automaton.

IV. PROPOSED METHODOLOGY

The proposed Architecture of linear feedback shift register is implemented by two modules:

- Modified clock scheme module
- Bit interchangeable module

A. Modified clock scheme module

Data_in	Data_out	Clock	Modified clock
1	0	1	1
0	1	1	1
1	1	1	0
0	0	1	0

TABLE 3.1 TRUTH TABLE FOR THE MODIFIED CLOCK

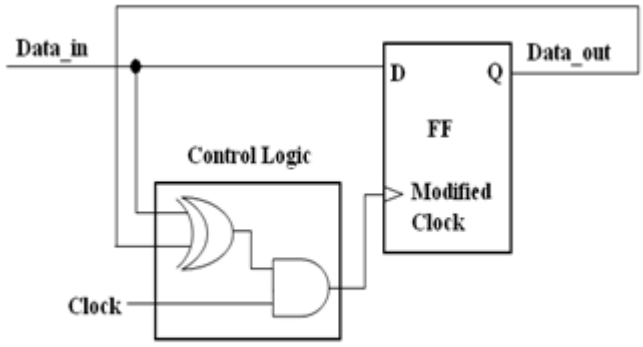


Figure 3.2 Switching unit of LFSR with Modified Clock

B. Bit Interchangeable Module

Based on the suggested bit interchanging methodology, the modified LFSR can be designed use with the conventional LFSR and a group of two-input multiplexers where bit n is considered as the selection line of the multiplexers.

.

V. MODIFIED ARCHITECTURE FOR 3-BIT LFSR

Here I was implemented 3-Bit Modified LFSR. The Architecture of 3-Bit modified LFSR is in figure 3.3.

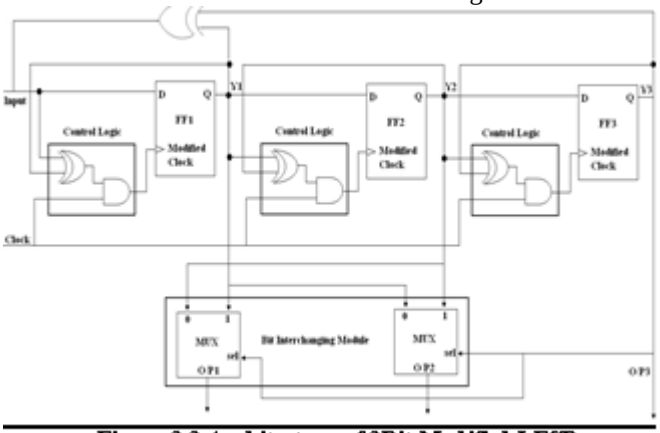
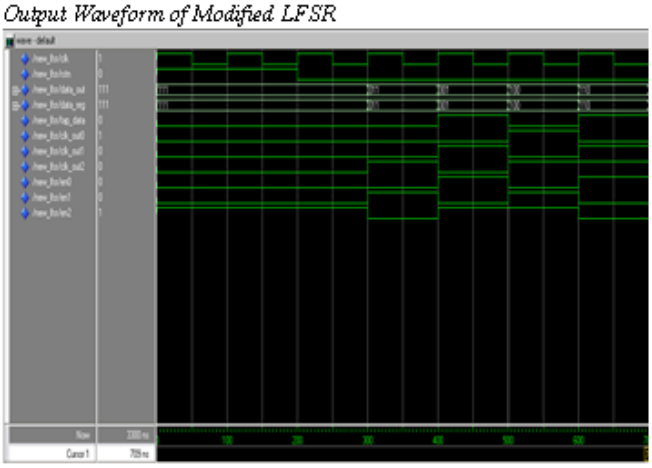


Figure 3.3 Architecture of 3Bit Modified LFSR

VI. SIMULATION AND SYNTHESIS RESULTS AND ANALYSIS

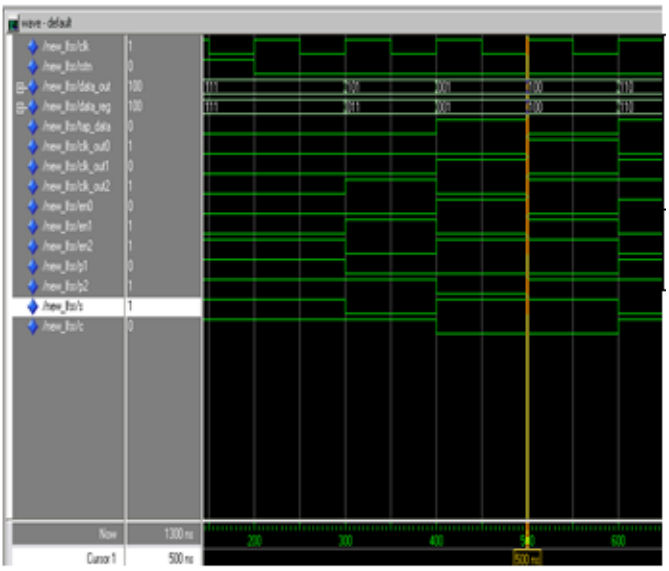
1. Results of Modified LFSR with Clock gating and Bit interchangeable module:

Output Waveform of Modified LFSR

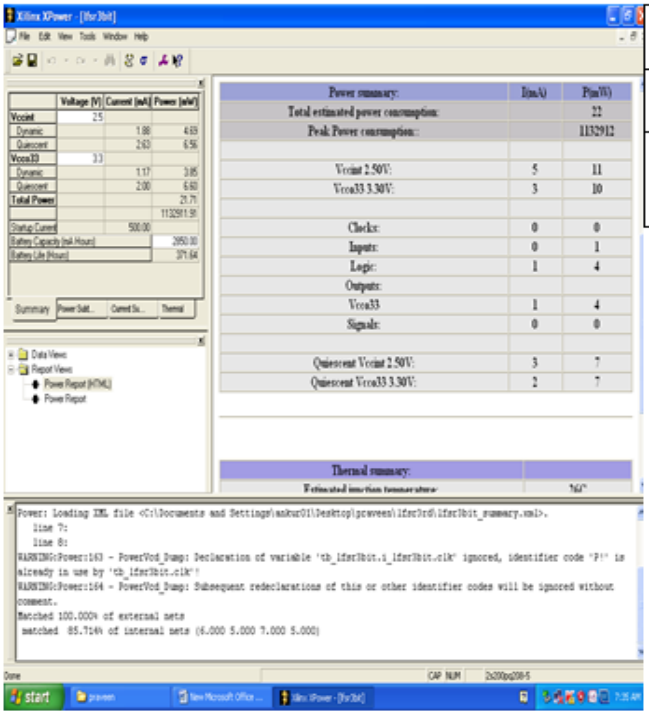


2. Results of Modified LFSR with CUT:

Output Waveform of Modified LFSR with CUT



1. POWER RESULT of 3-Bit conventional LFSR



VII. EXPRIMENTAL RESULT AND ANALYSIS

Test vectors are actually the same but their order of scan shifting changes. The THD reduction acquired with maximal length LFSRs is presented in Table 4.1

TABLE 4.1 TOTAL HAMMING DISTANCE REDUCTION

Maximal length LFSR	THD without Order	THD with order	THD Reduction (%)
3-bit LFSR	11	9	18.18

TABLE 4.2 TOTAL POWER CONSUMPTION OF CONVENTIONAL LFSR AND LFSR WITH MODIFIED CLOCK.

LFSR Designs	Total power consumption (mW)
Conventional LFSR	22mW
LFSR with modified clock	17mW

VIII. CONCLUSION

This paper presented a new low-power LFSR to reduce the average and peak power of a digital circuit during the testing mode. By increasing the correlation between the test pattern in circuit, the switching activity in the circuit under test therefore the power consumption is reduced. Additional intermediate test patterns inserted hold between the original random patterns reduces the average and peak power, but do not effect on fault coverage. The Power Consumption with modified LFSR is **17mW**. So power saving is about **22%** then the conventional LFSR.

REFERENCES

[1] Bei Cao, Liyi Xiao, Yongsheng Wang" A Low Power Deterministic Test Pattern Generator for BIST Based on LFSR," Electronic Design, Test and Applications, DELTA 2008. 4th IEEE International Symposium,pp-266-269,2008

[2] P.Girard, C.landrault, S.Pravossoudovitch, D Severac, "Reducing Test power Consumption During Test Vector Ordering" IEEE International Symposium on Circuits and Systems, 1998.

[3] V.D. Agrawal and M. Bushnell, Essentials of Electronic Testing For Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.

[4] N.Ahmed, M. H. Tehranipour, M. Nourani, "Low Power Pattern Generation for BIST Architecture", IEEE Circuits and Systems, 2004. ISCAS '04. Proceedings of the International Symposium, 23-26 May 2004, Vol. 2, pages 689-92., 2004

[5] M. Bellos, D. Bakalis, D.Nikolos, X. Kavousianos, "Low Power Testing by vector Ordering with Vector Repetition", pp 205-210,2004.

[6] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, "A Gated Clock Scheme for Low Power Scan-Based BIST" Proceedings of the Seventh IEEE International On-Line Testing Workshop (IOLTW'01), 2001.

[7] Walter Aloisi and Rosario Mita, Member, IEEE, Gated clock design of Linear Feedback Shift Register , IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 55, NO. 6, JUNE 2008.

[8] Deterministic and Low Power BIST Based on Scan Slice Overlapping, Ji Li Yinhe Han Xiaowei Li, Proc.of NSFC, pp. 5670-5673, 2005.

[9] L. Jie, Y. Jun, L. Rui, and W. Chao, "A new BIST structure for low power testing," Proc. International ASIC/SOC Conference, pp.1183– 1185, 2003.

[10] P. Girard, "Survey of low-power testing of VLSI circuits," Proc. Design and Test of Computers, IEEE Press, Volume 19, Issue 3, May-June 2002, Page(s) 80-90.

[11] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, H. -J. Wunderlich, "A modified Clock

Scheme for a Low Power BIST Test Pattern Generator," in Proc. *VLSI Test Symp. (VTS'01)*, pp. 306-311, 2001.

[12] Kicheol KIM, Dongsub SONG, Incheol KIM, and Sungho KANG, "A New Low Power Test Pattern Generator for BIST Architecture," Proc.IEICE TRANS. ELECTRON., VOL.E88–C, NO.10 OCTOBER 2005.

[13] Abdallatif S. Abu-Issa and Steven F. Quigley, "LT-PRPG: Power Minimization Technique for Test-Per-Scan BIST", International Conference on Design & Technology of Integrated Systems in Nanoscale Era, proc. pp. 1-5, 2008.

[14] F. Corno et al., "Low Power BIST via Non-Linear Hybrid Cellular Automata," Proc. 18th VLSI Test Symp. (VTS 00), IEEE CS Press, Los Alamitos, Calif., 2000.

[15] X. Zhang, K. Roy, and S. Bhawmik, "POWERTEST: A Tool for Energy Conscious Weighted Random Pattern Testing," Proc. 12th Int'l Conf. VLSI Design, IEEE CS Press, Los Alamitos, Calif., 1999

[16] R. Madhusudhanan, R.Balarani "A BIST TPG for Low Power Dissipation and High Fault Coverage" International journal of mc square scientific research, Vol 1 , June 2009

[17]Sabir Hussain1 K Padma Priya "Test Pattern Generator (TPG) for Low Power Logic Built In Self -Test (BIST)" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

Vol. 2, Issue 4, April 2013

[18].Prathyusha Nayineni, S.K. Masthan Jayamukhi."Power optimization of BIST circuit using low power LFSR", International Journal of Computer Trends and Technology- volume 2 Issue2- 2011.